

Project Name :GM7MxxP

Platform : CFL-HR+N18E-GXR

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4. POWER MAP
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6. CPU CFL-H eDP/PEX/DMI/RSVD
7. CPU CFL-H MISC/CLK/JTAG/CFG
8. CPU CFL-H VCORE
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23. N/A
24. EC(IT5571E)/KB CONN
25. N/A
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27. LAN(RTL8111G-CG)
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36. POWER VCORE/VCCGT/VCCSA
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38. POWER +1.8VA/+1.05VA\_PCH
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40. POWER +VCCIO/+VS PWR/+V PWR

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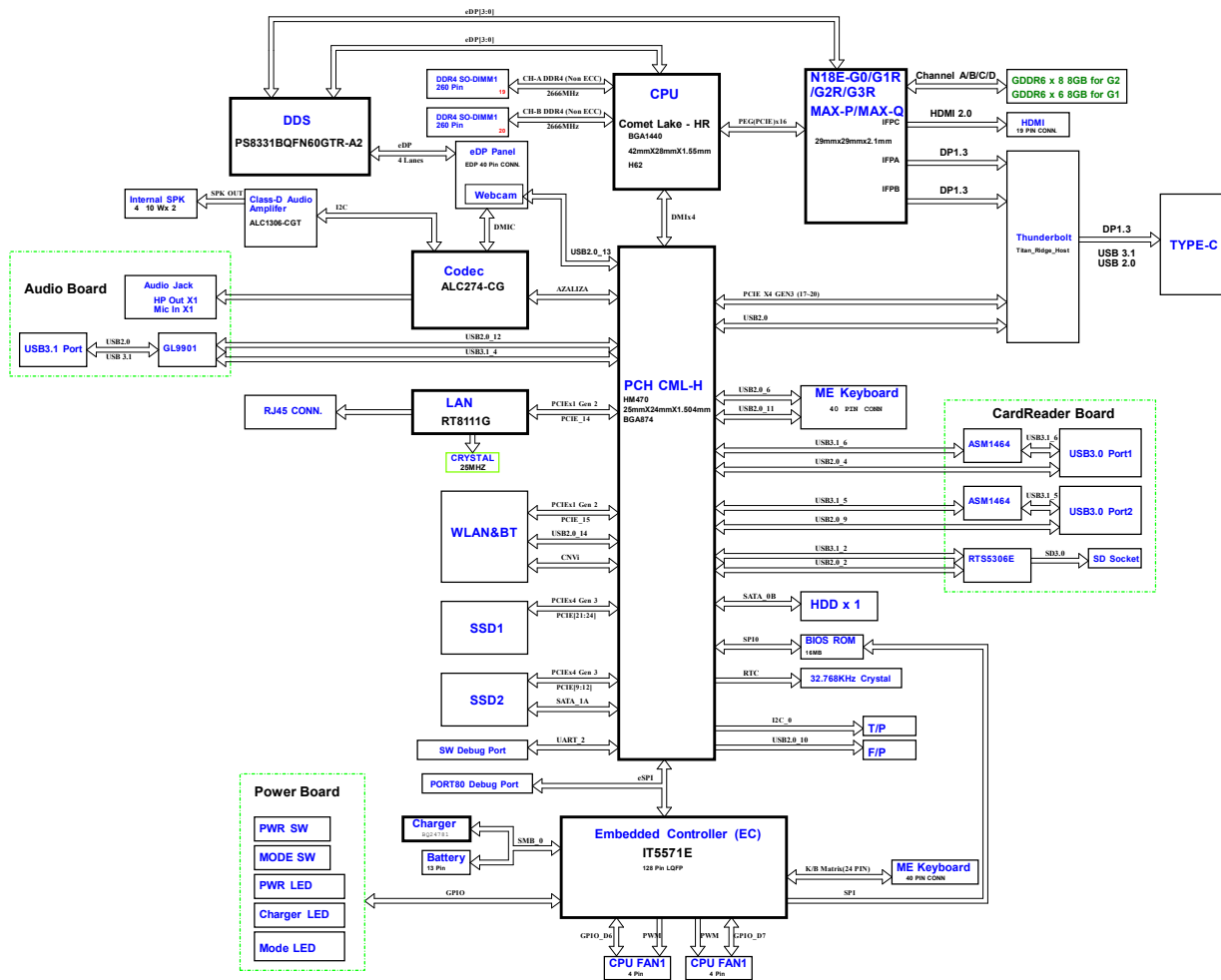
M/B Schematic Version Change List

Release Date	Version	PCB P/N	PCB Description	PCBA P/N	Note

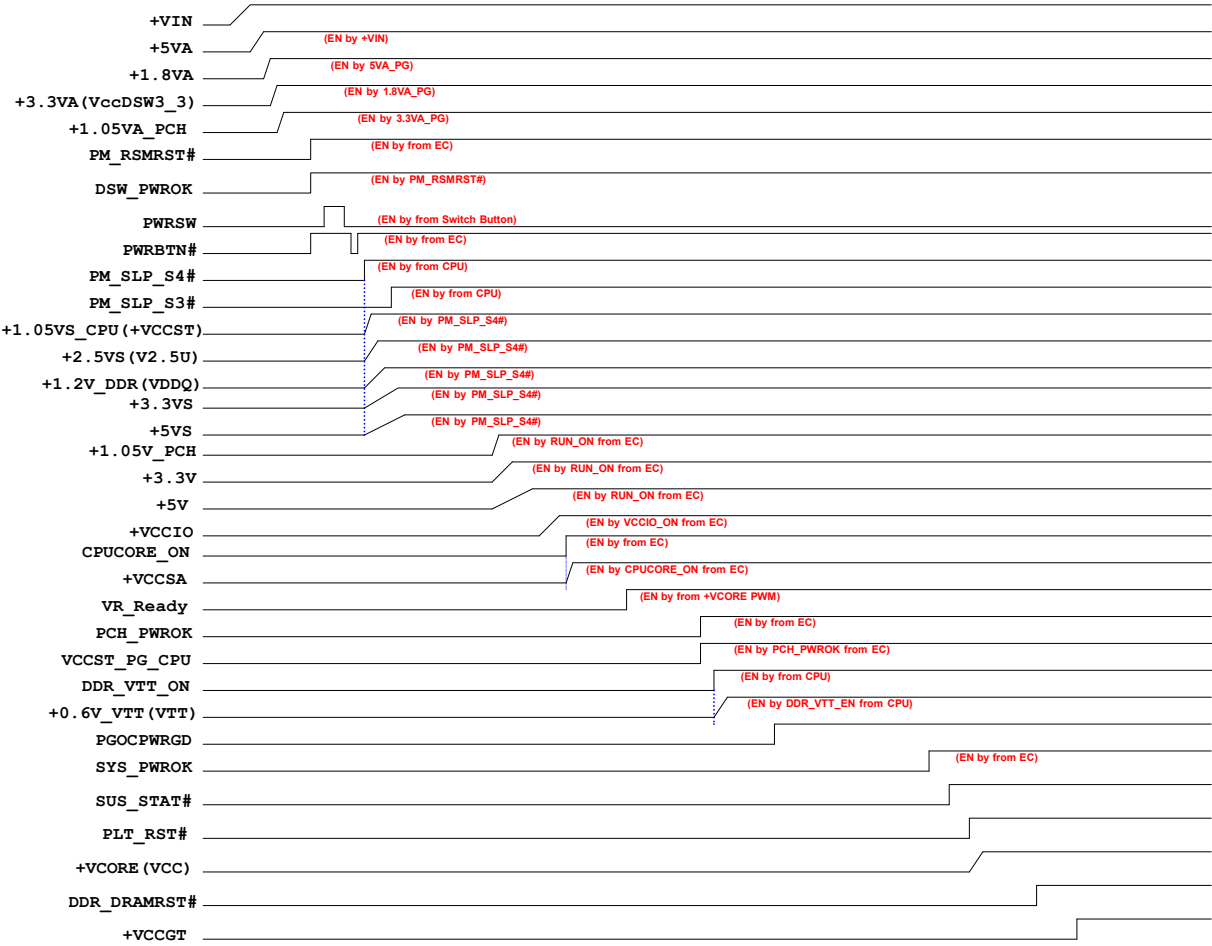
Daughter Board Schematic Version Change List

Release Date	Version	PCB P/N	PCB Description	PCBA P/N	Note

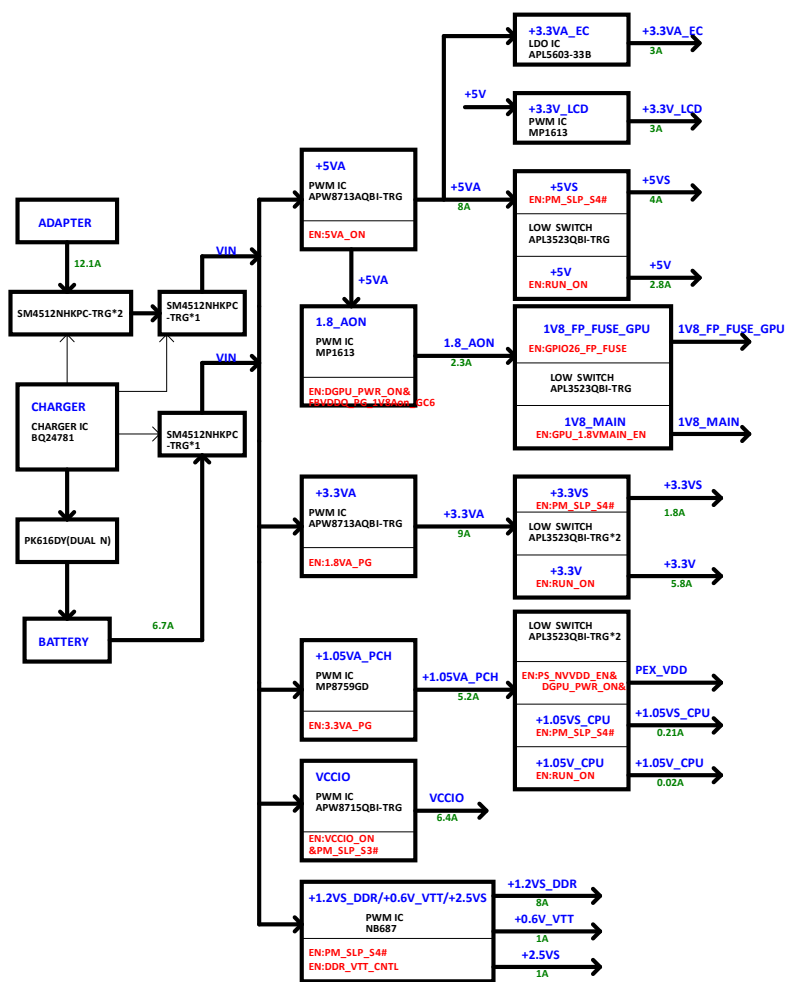
## SYSTEM BLOCK DIAGRAM



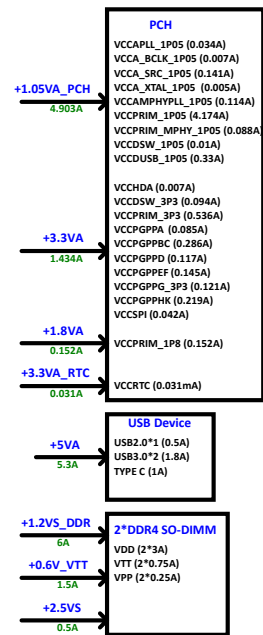
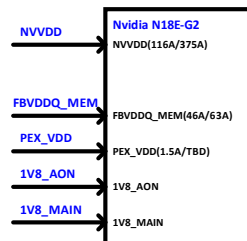
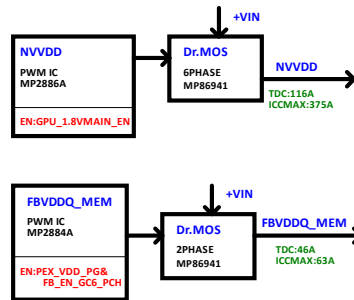
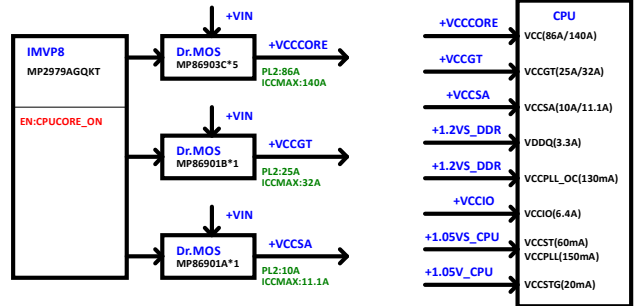
POWER ON SEQUENCE



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Doc	03_POWER SEQUENCE		
Doc	Document Number	GM7MGxx	
Doc	Version	1.0	A

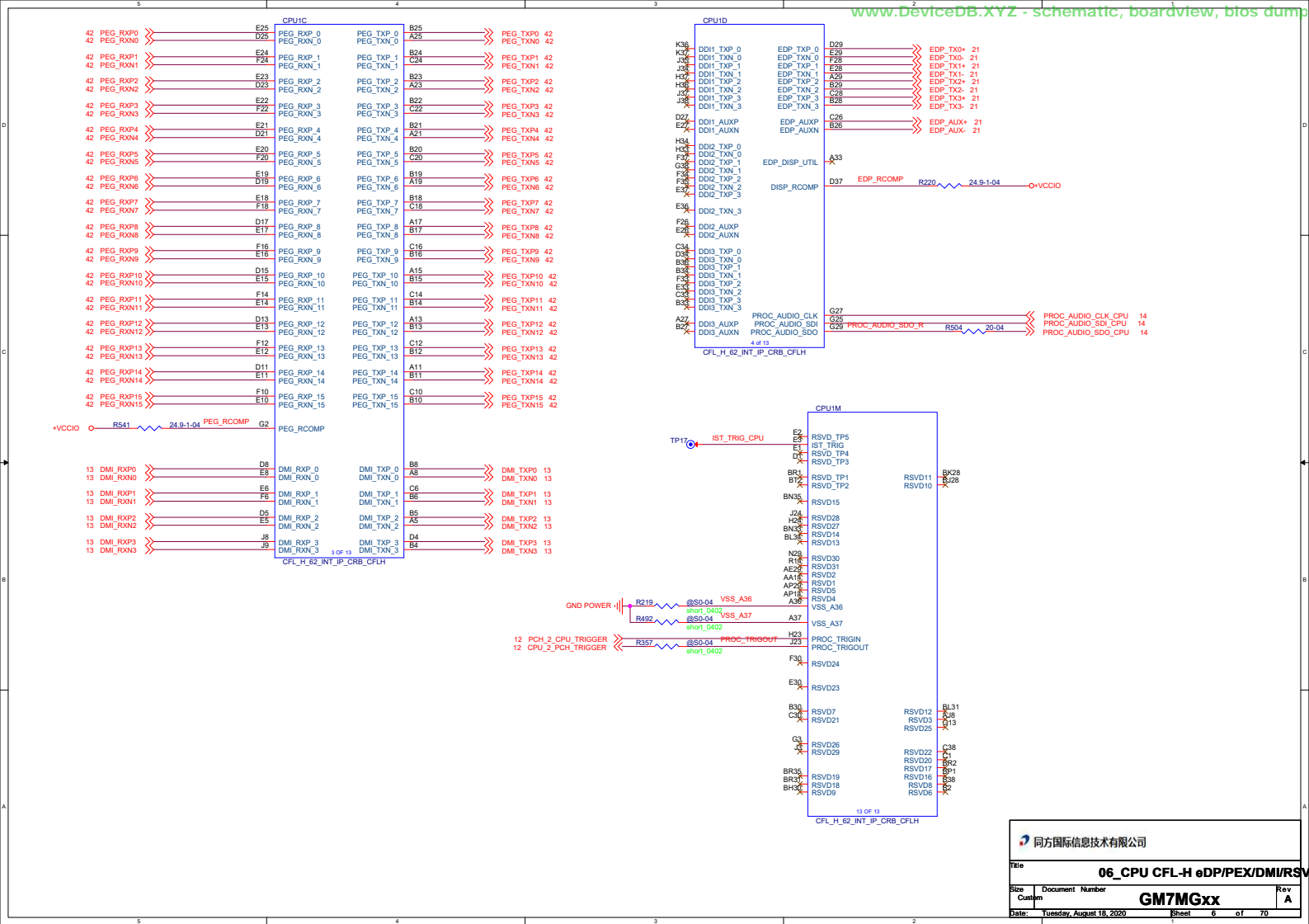


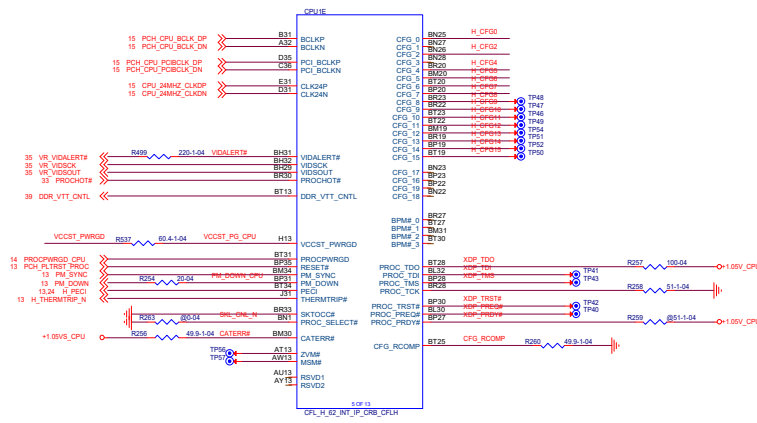
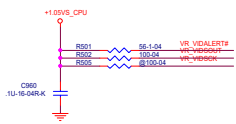
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	04_POWER MAP	GM7MGxx	A
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H_CFG0 (IPU)	Stall reset sequence after PCU PLL lock until de-asserted
0	Stall
1	Normal Operation No stall (Default)

H\_CFG0 R511 10K-1.04

H_CFG2 (IPU)	PCI Express* Static x16 Lane Numbering Reversal
0	Lane numbers reversed
1	Normal operation

H\_CFG2 R507 10K-1.04

H_CFG4 (IPU)	eDP Presence strap
0	Enabled
1	Disabled

H\_CFG4 R501 10K-1.04

H_CFG6 (IPU)	H_CFG5 (IPU)	PCI Express* Bifurcation
0	0	1x8, 2x4 PCI Express
0	1	reserved
1	0	2x8 PCI Express
1	1	1x16 PCI Express

H\_CFG5 R515 10K-1.04

H\_CFG6 R502 10K-1.04

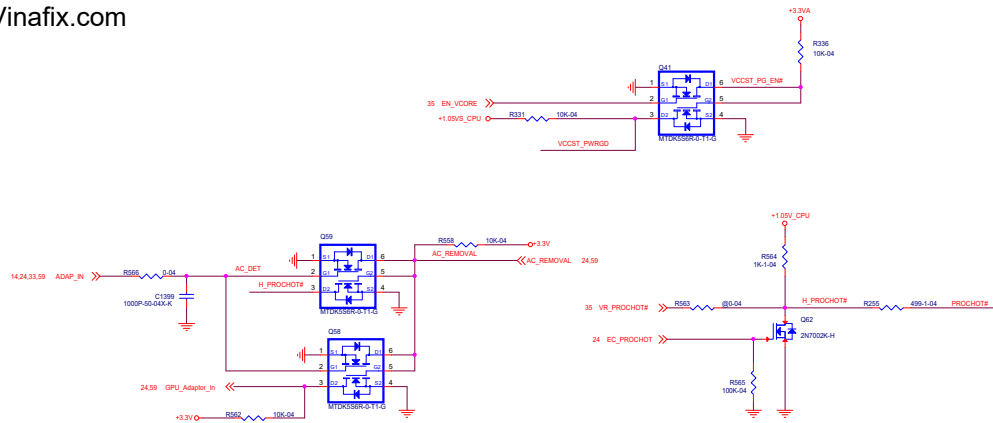
H_CFG7 (IPU)	PEG Training
0	PEG Wait for BIOS for training
1	PEG Train immediately following RESET# de assertion (Default)

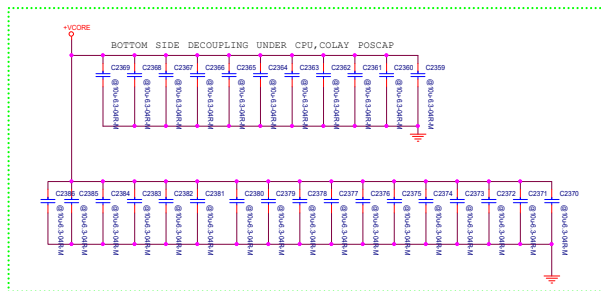
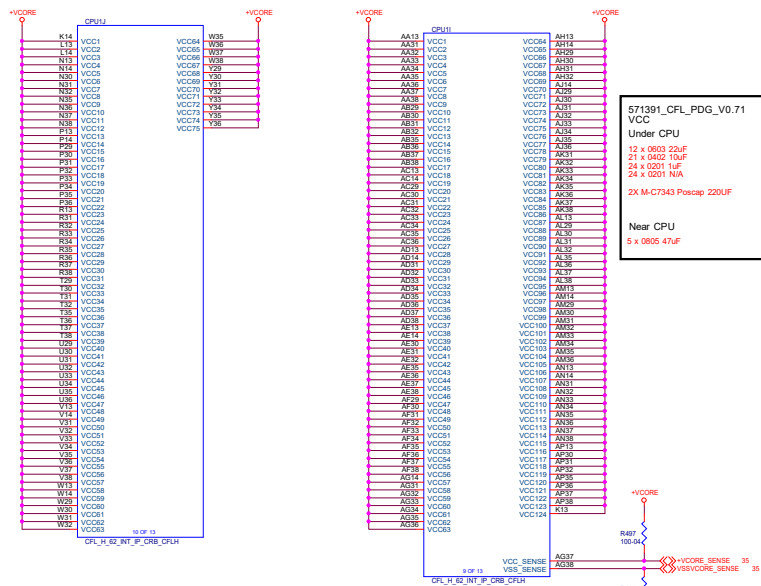
H\_CFG7 R527 10K-1.04

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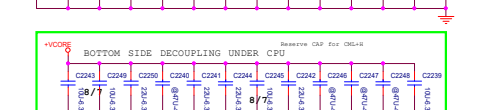
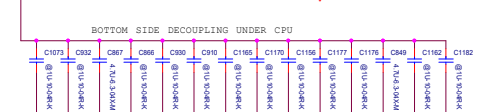
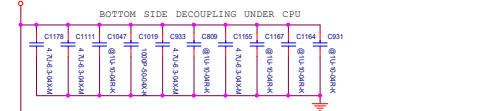
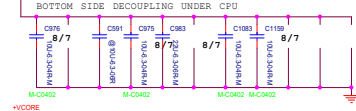
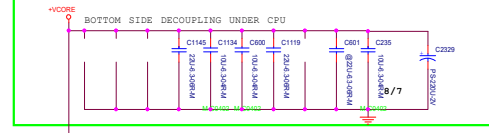
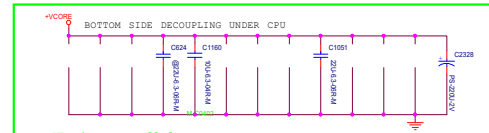
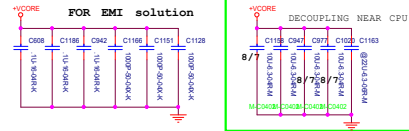
Doc	Document Number	Rev
07	CPU CFL-H MISC/CLK/JTAG/CFL	A
GM7MGxx		
Date	Tuesday, August 18, 2020	Print 7 of 76

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## FOR EMI solution



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Doc: 08\_CPU CFL-H VCCORE  
Rev: A  
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611586\_CML\_H\_PDG\_Rev0p9  
VccIO  
Bulk Decoupling Example  
Processor Decoupling Requirements

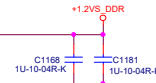
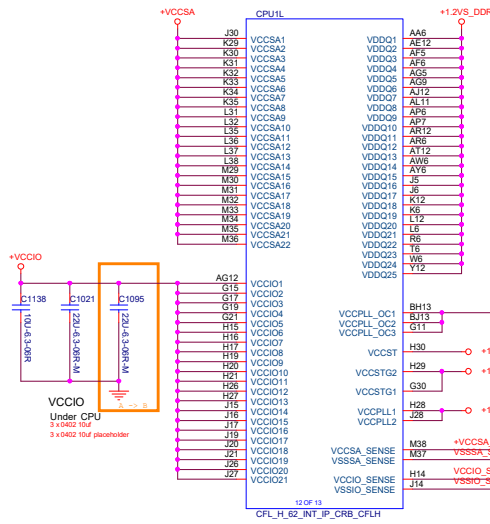
611586\_CML\_H\_PDG\_Rev0p9  
VccSA  
Bulk Decoupling Example  
Processor Decoupling Requirements

611586\_CML\_H\_PDG\_Rev0p9  
Processor Decoupling Requirements  
VDDQ  
VccSTG  
VccPLL  
VccPLL\_OC

VccIO  
Page 10 : 22u\*2 + 10\*1 = 54uF  
Page 40 : 22u\*4 = 88uF  
Total : 142uF (CML-H spec : 124uF)

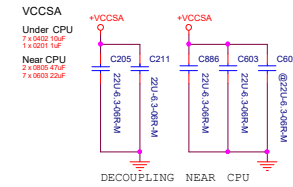
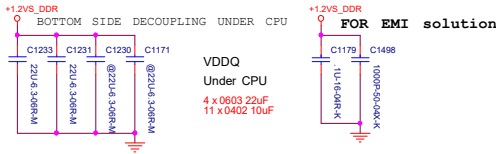
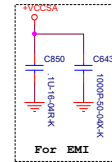
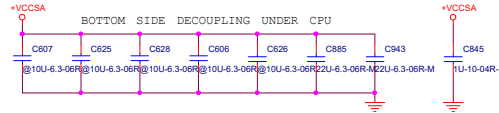
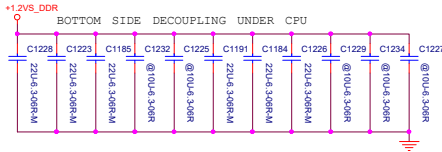
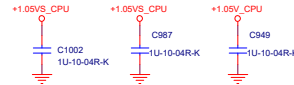
VccSA  
Page 10 : 47u + 12 = 59uF  
Page 36 : 22u + 4 = 26uF  
Total : 85uF (spec : 523uF)

VDDQ  
Page 10 : 22u \* 15 = 330uF  
Total : 330uF (spec : 198uF)

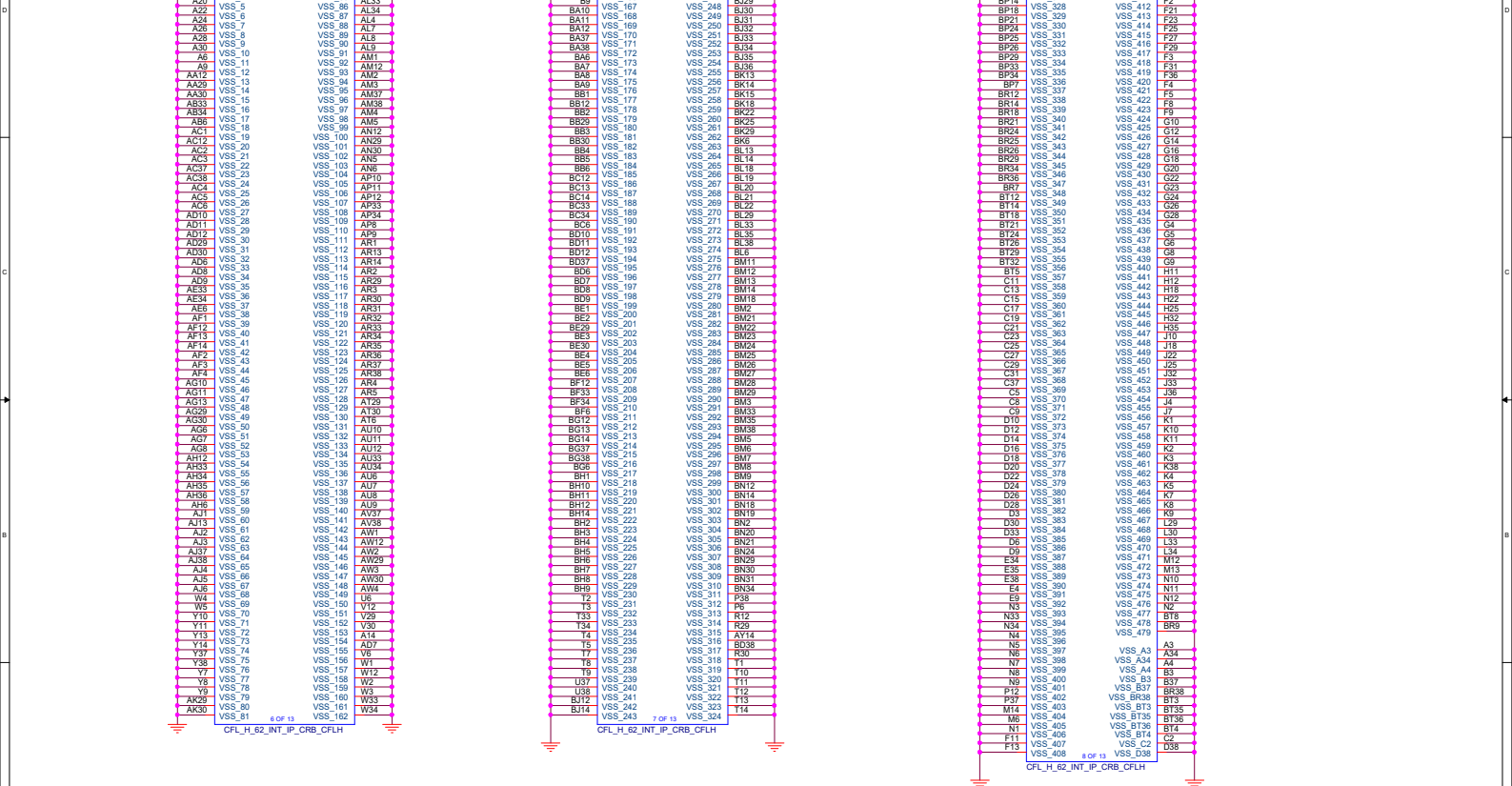


VCCSTG  
Under CPU  
1x 0201 1uF  
VCCSTG  
Under CPU  
1x 0201 1uF  
VCCPLL\_OC  
Under CPU  
2x 0201 1uF

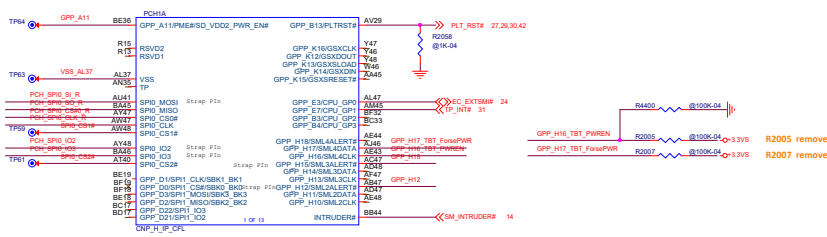
VCCPLL\_OC:  
CPU digital PLL power rails  
VCCPLL:  
CPU PLL power rails  
VCCSTG:  
Sustain voltage for processor  
in Standby modes  
VCCSTG:  
Gated version of VCCSTG  
(1)VCCPLL is allowed to be OFF in S3,  
but it is generally assumed to be ON  
since it is powered from the same  
source as VCCSTG.  
(2) VCCPLL\_OC is allowed to be turned  
off during S3 if it is not powered  
directly from VDDQ



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Title			
10_CPU CFL-H VCCSA/VCCIO/VDDQ			
Size			
Custom			
Date: Tuesday, August 18, 2020			
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Rev A			



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Title 11_CPU CFL-H GND	
Size Custom	Document Number GM7MGxx
Date: Tuesday, August 18, 2020	Sheet 11 of 70



GPP\_H15  
External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V.

GPP\_H15 R344 100K-04 Q=3.3V

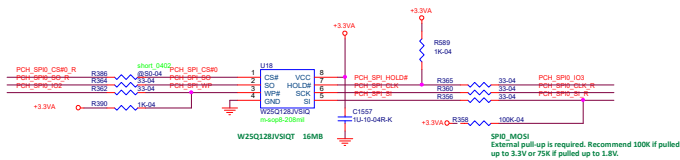
GPP_H12	eSPI Flash Sharing Mode
0	Master Attached Flash Sharing (MAFS) enabled (Default)
1	Slave Attached Flash Sharing (SAFS) enabled

GPP\_H12 R344 100K-04 Q=3.3V

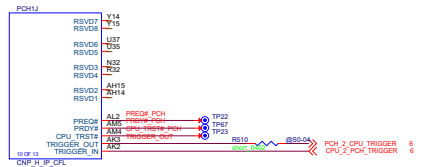
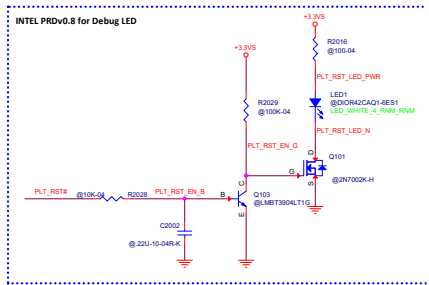
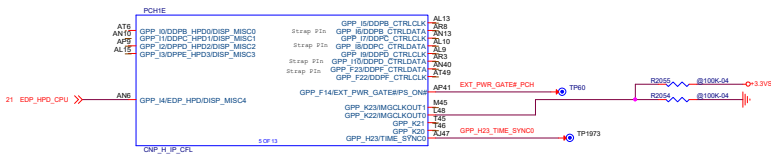
to eSPI EC

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to eSPI EC



8/18 del U1922



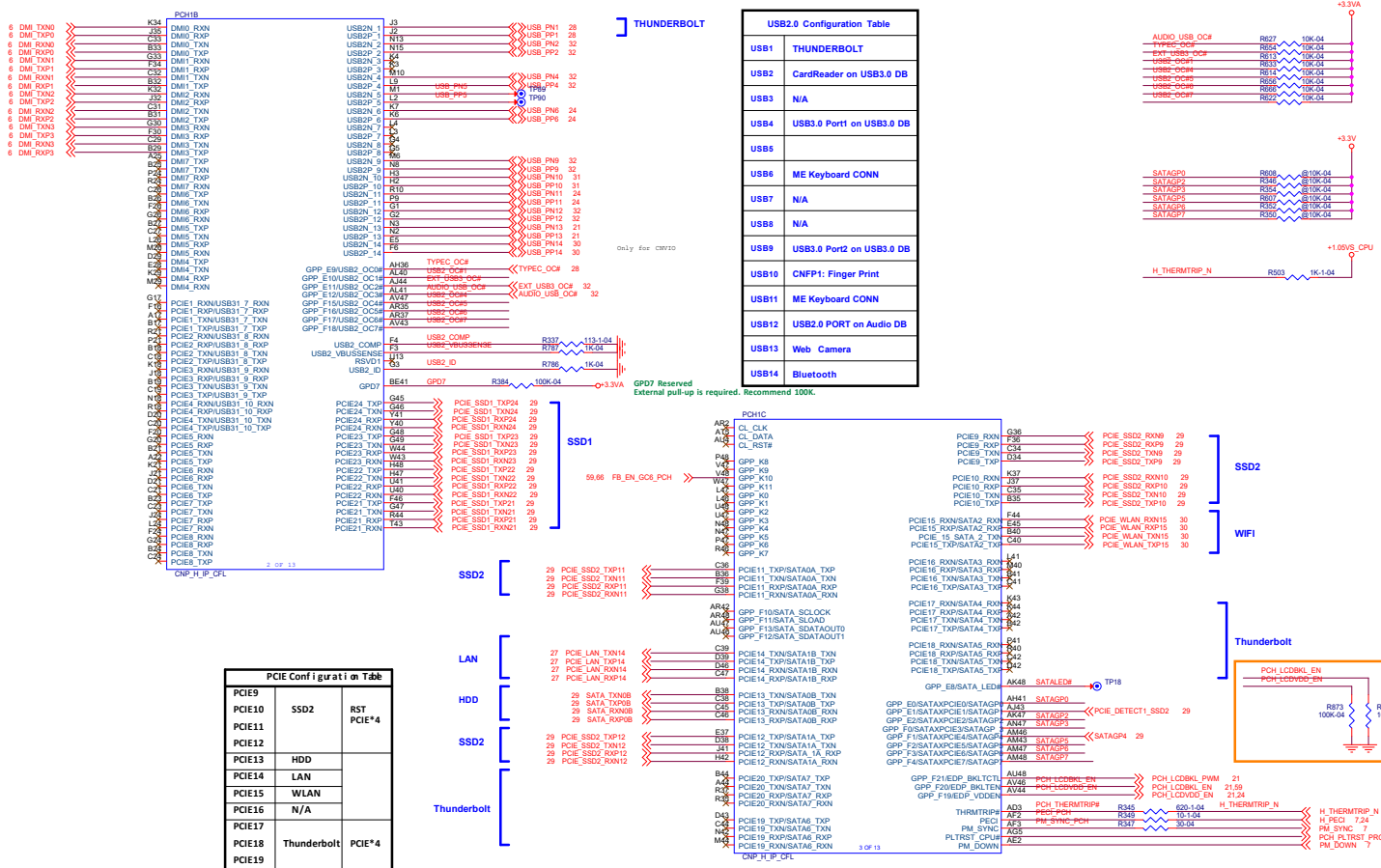
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12\_PCH CFL-H SPVDDI CTRL/RSVD

GM7MGxx

Version: 1.0

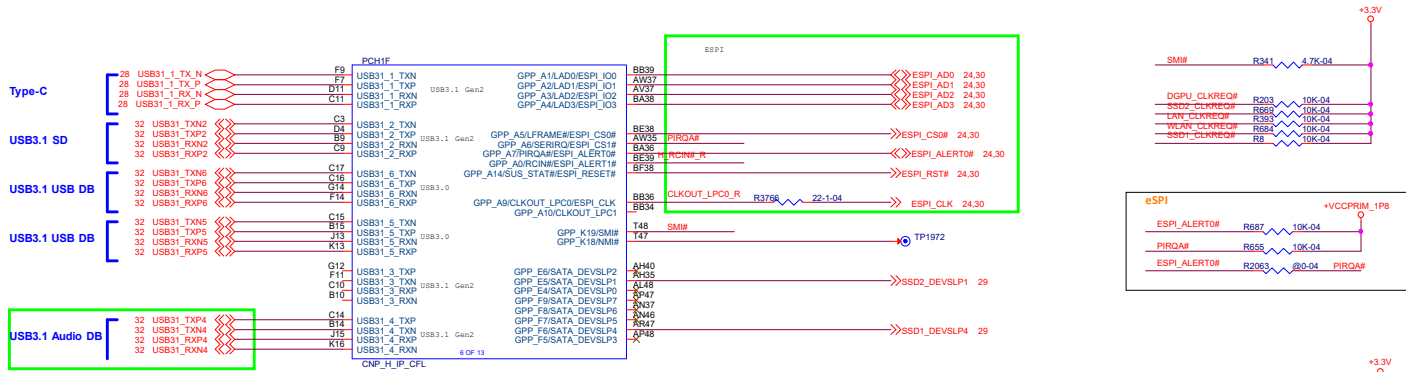
Rev: A



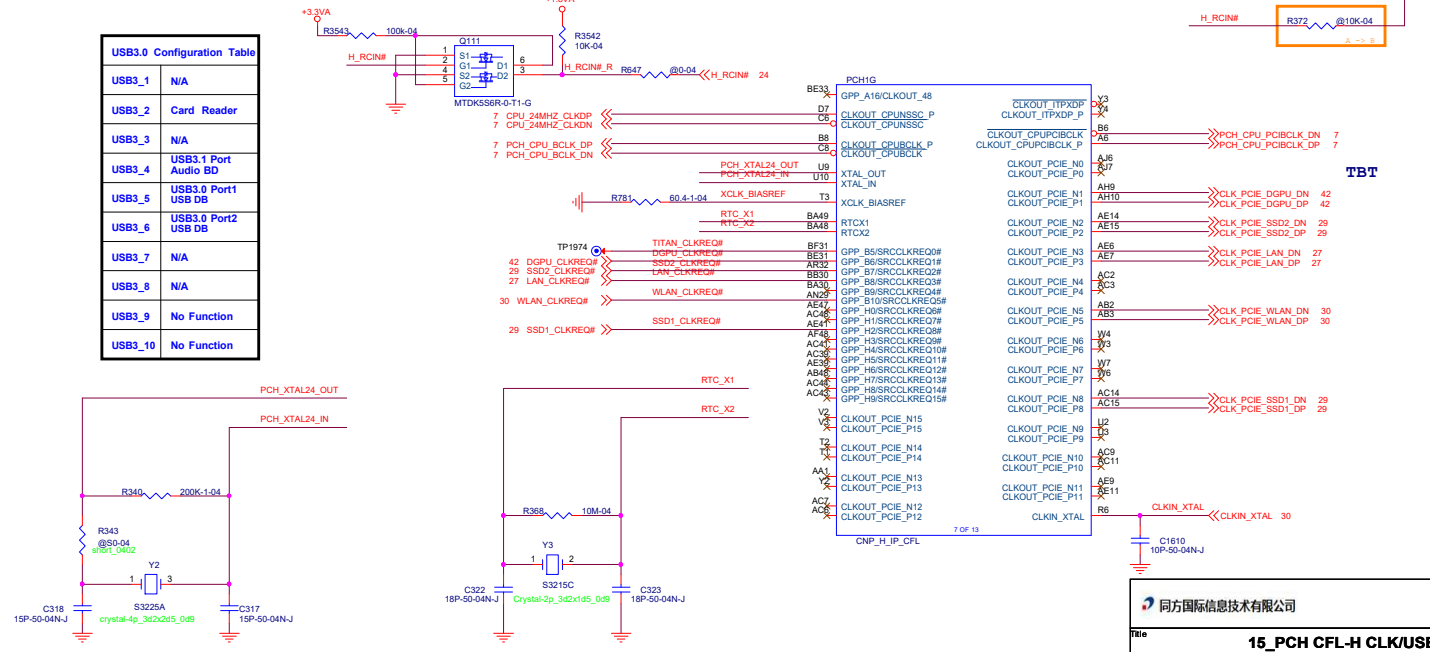
PCIe Configuration Tab			
PCI9			
PCI10	SSD2	RST	PCI4
PCI11			
PCI12			
PCI13	HDD		
PCI14	LAN		
PCI15	WLAN		
PCI16	N/A		
PCI17			
PCI18	Thunderbolt	PCI4	
PCI19			
PCI20			
PCI21			
PCI22	SSD1	RST	PCI4
PCI23			
PCI24			

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13_PCH CFL-H DM/PCIE/USB2/SATA			
Doc Number	GM7MGxx		Rev A
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USB3.0 Configuration Table	
USB3_1	N/A
USB3_2	Card Reader
USB3_3	N/A
USB3_4	USB3.1 Port Audio BD
USB3_5	USB3.0 Port1 USB DB
USB3_6	USB3.0 Port2 USB DB
USB3_7	N/A
USB3_8	N/A
USB3_9	No Function
USB3_10	No Function

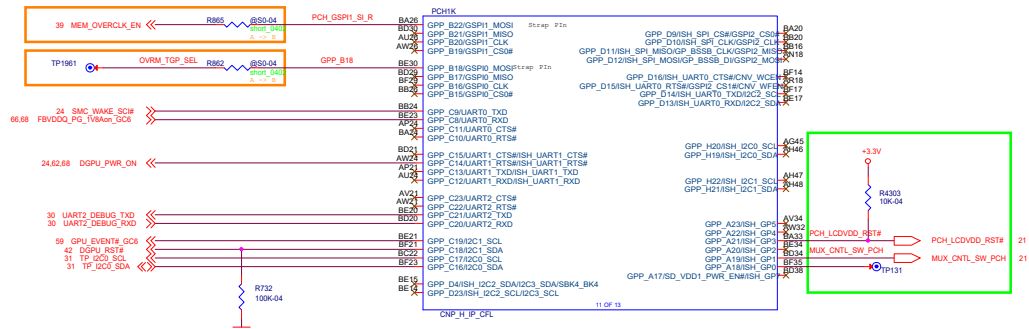


GPP_B22/GSPI1_MOSI(IPD)	Boot BIOS Destination
0	SPI (Default)
1	LPC

+3.3V R864 @150K-04 PCH\_GSPI1\_SL\_R

GPP_B18/GSPI0_MOSI(IPD)	No Reboot Mode with TCO Disabled
0	Disabled (Default)
1	Enable

+3.3V R573 R574 @4.7K-04 GPP\_B18

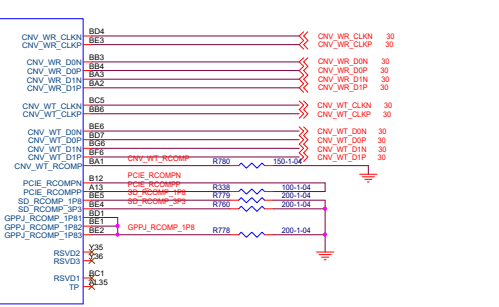
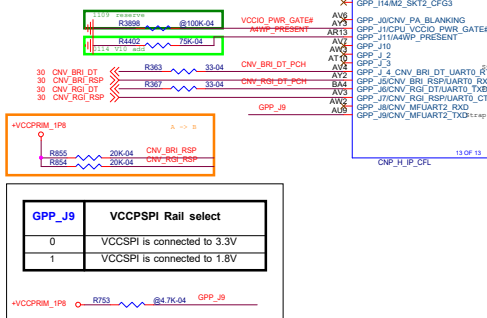


CNV_BRI_DT (IPD)	XTAL Frequency Select
0	38.4MHz XTAL frequency
1	24MHz XTAL frequency (Default)

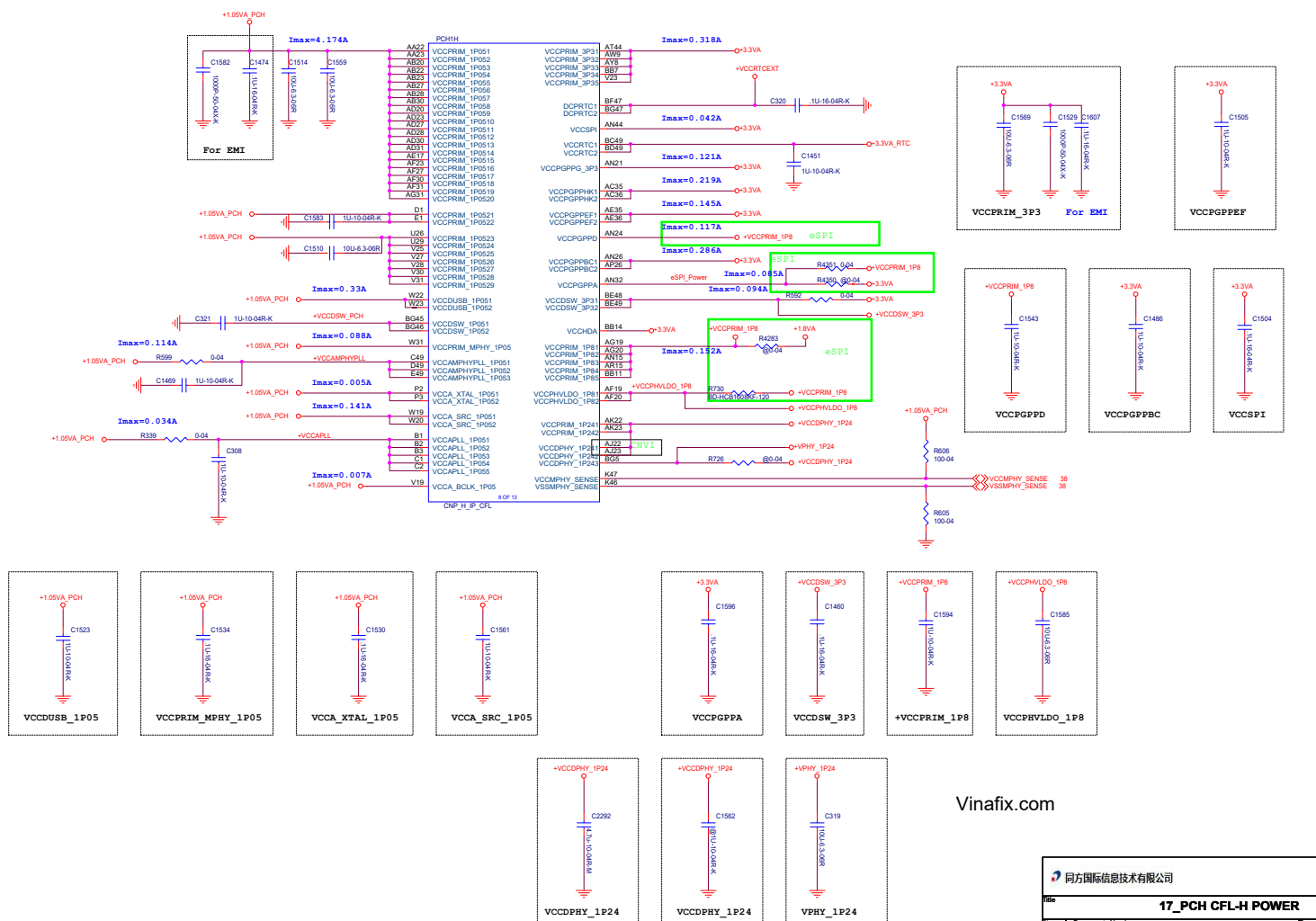
+VCCPRIM\_1P8 R796 @10K-04 CNV\_BRI\_DT\_PCH

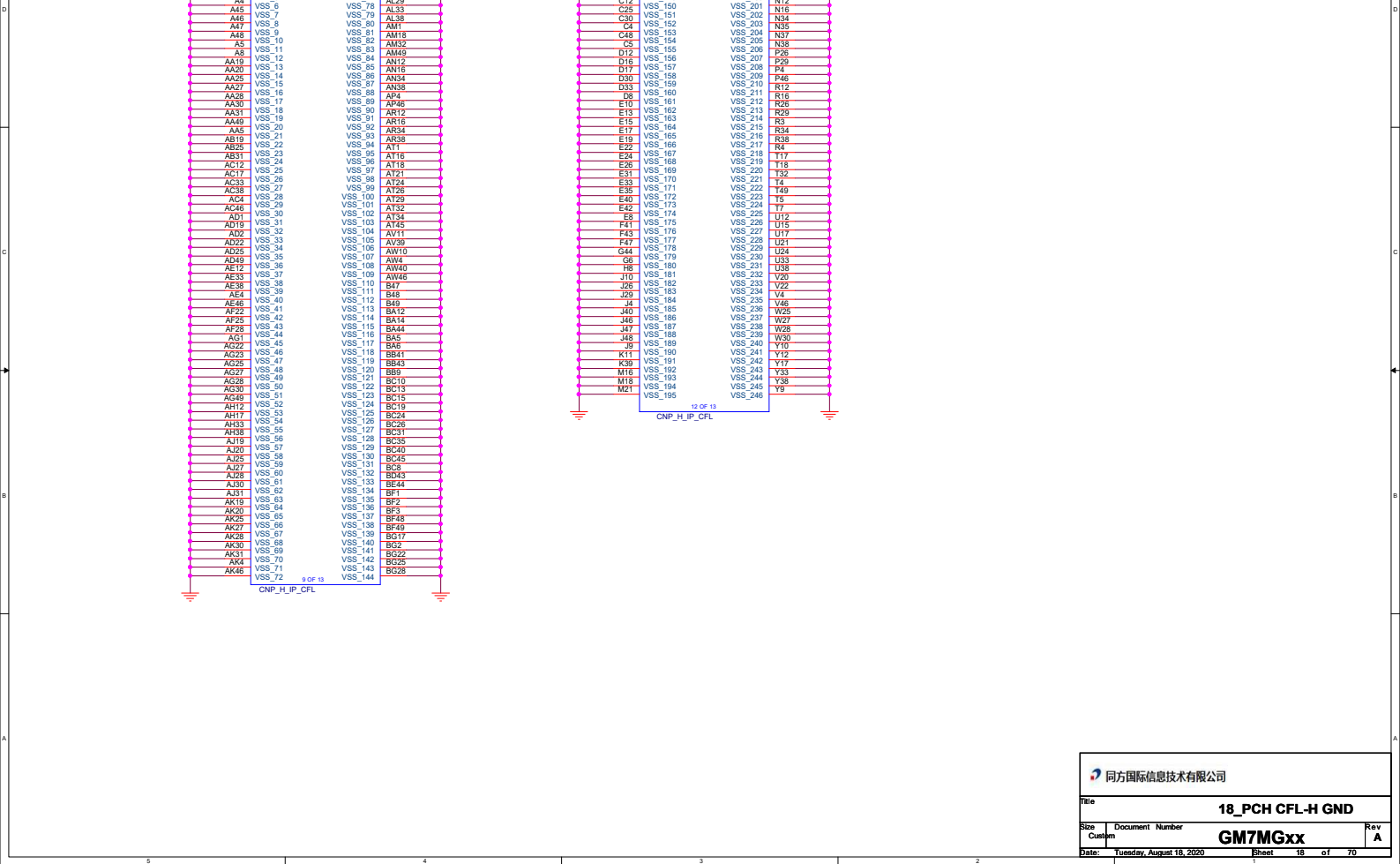
CNV_RGI_DT	M.2 CNV Mode Select
0	Integrated CNVi enable
1	Integrated CNVi disable

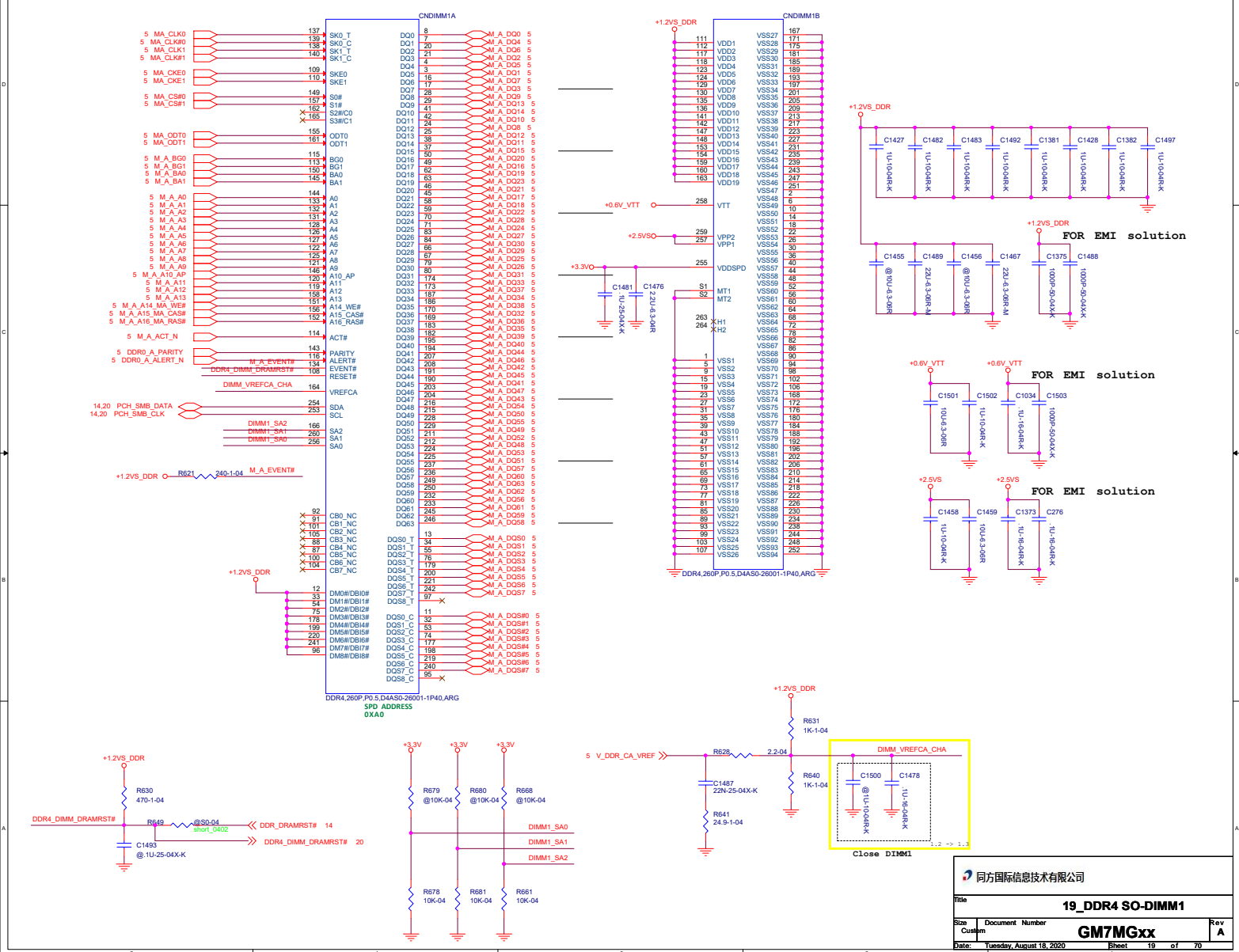
+VCCPRIM\_1P8 R795 @20K-04 CNV\_RGI\_DT\_PCH  
Close to CNVi module

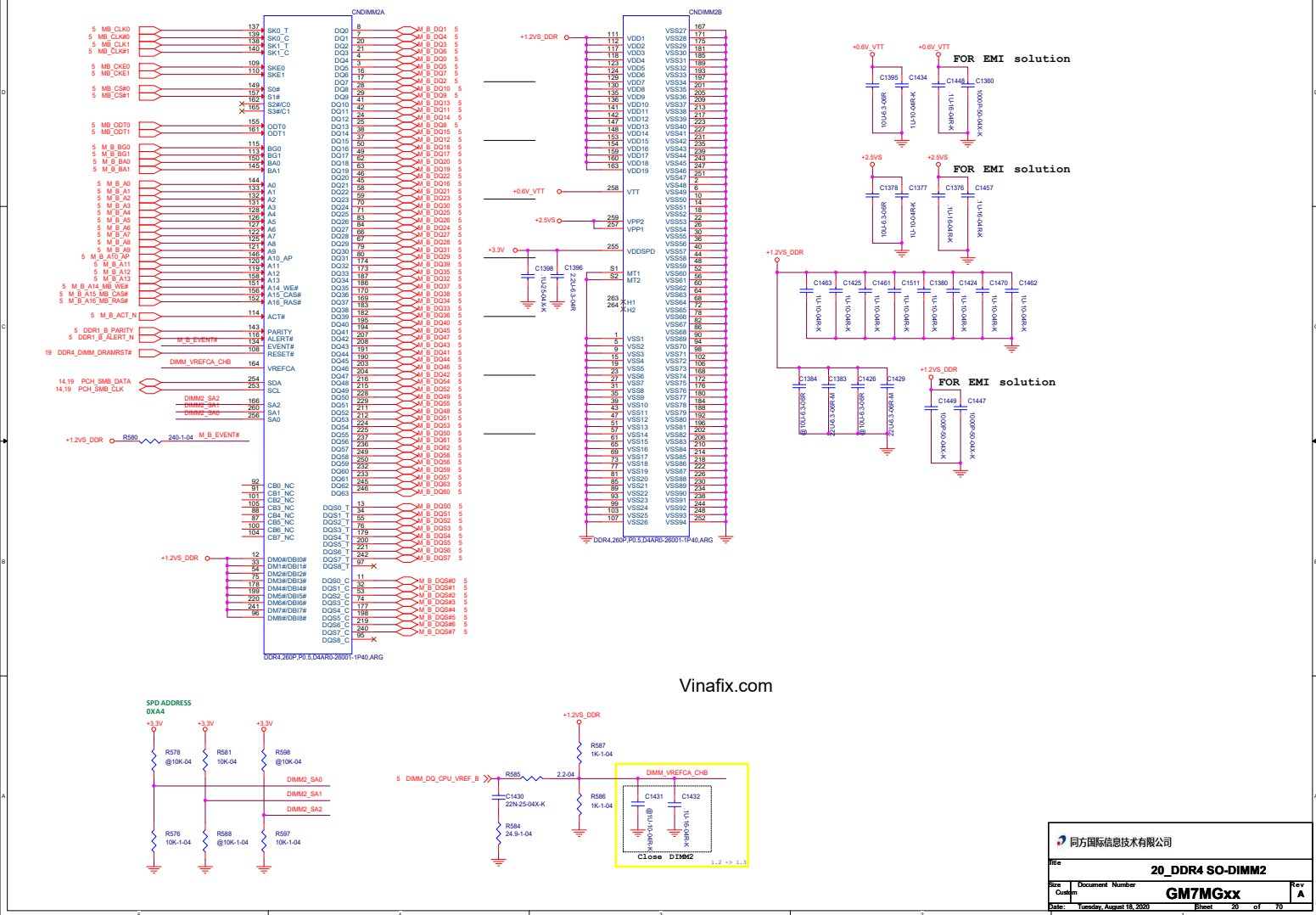




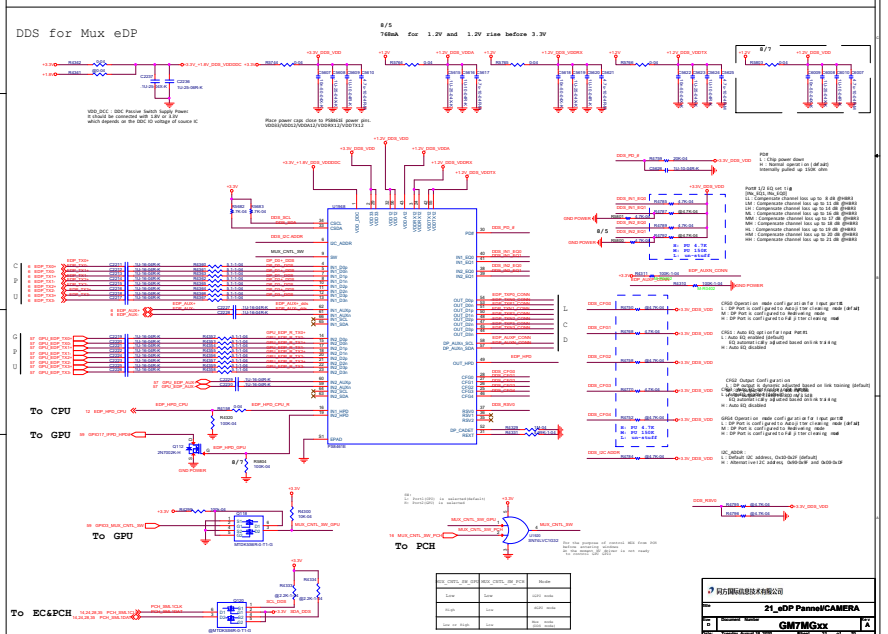
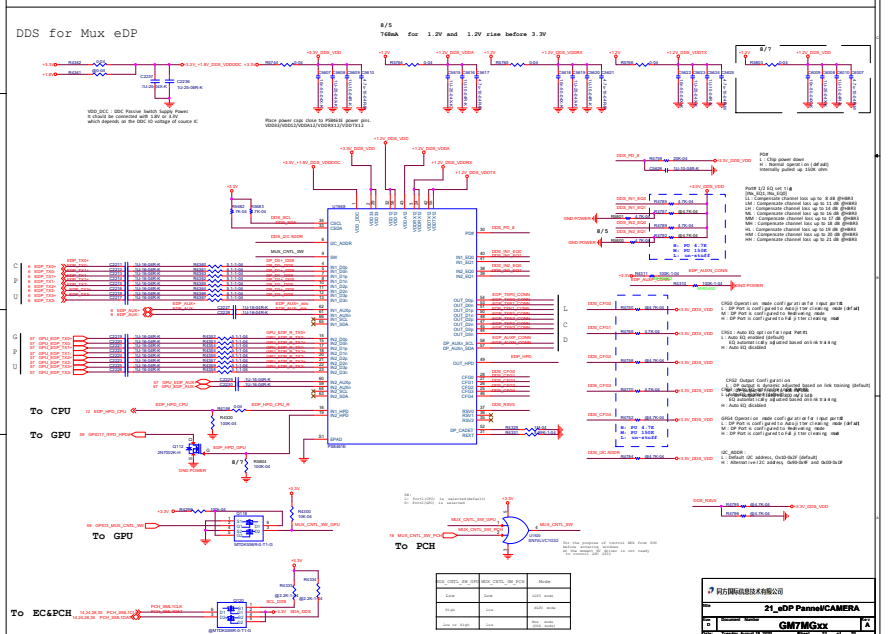
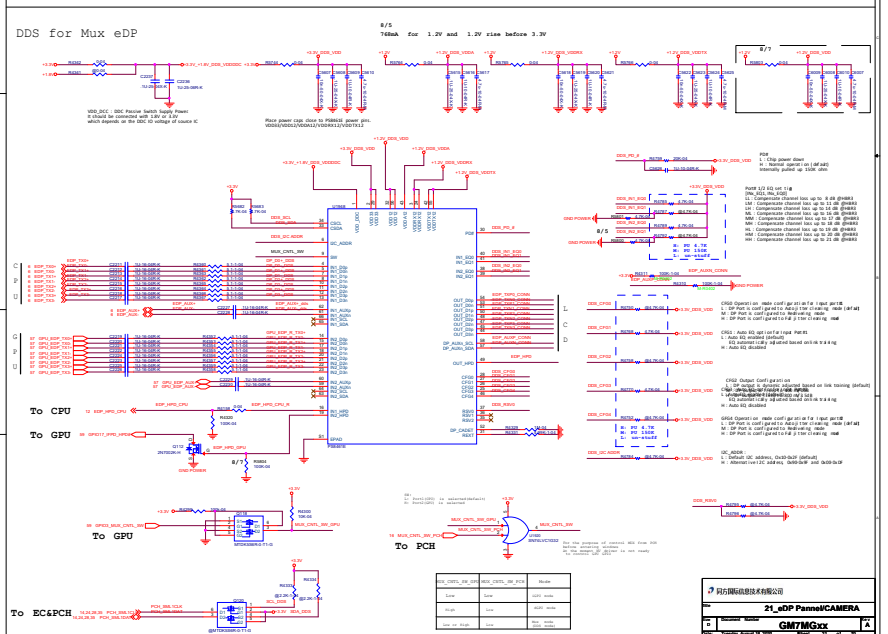
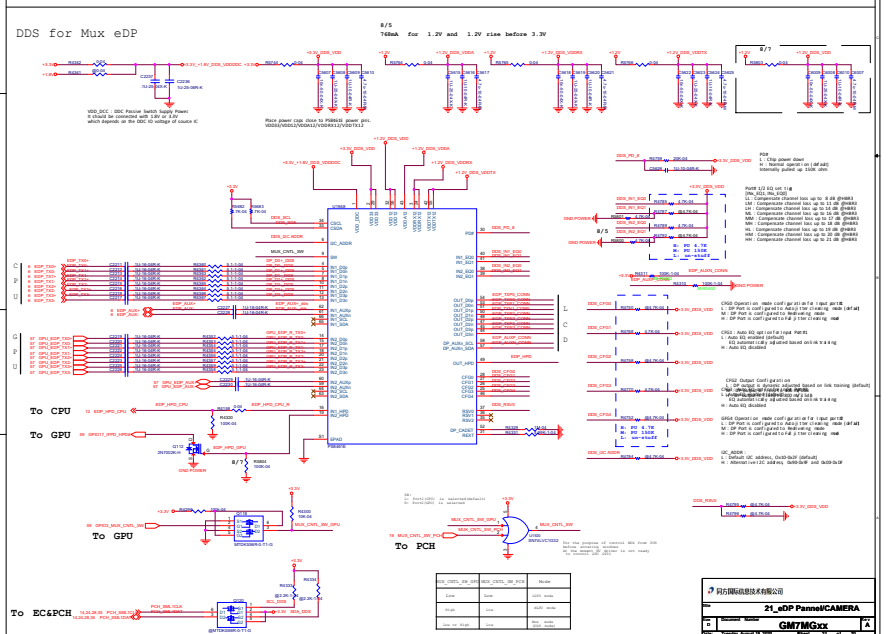
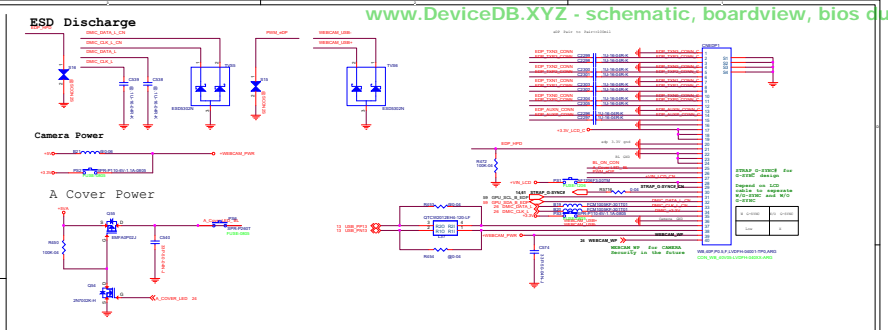






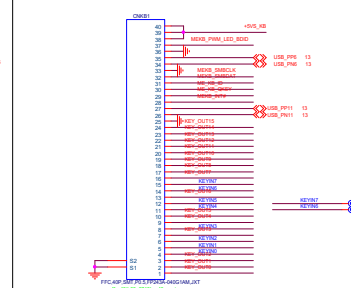
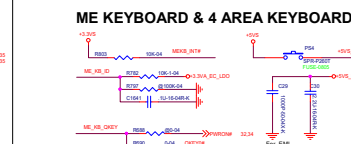
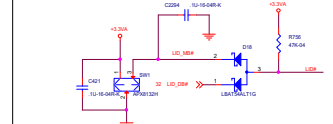
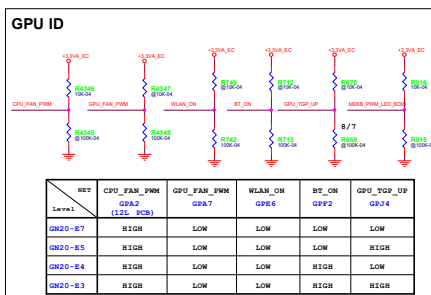
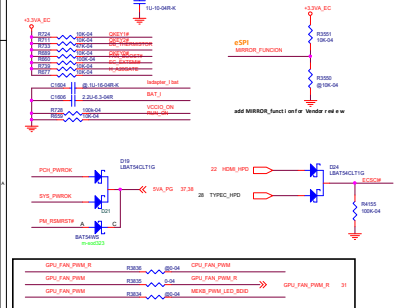
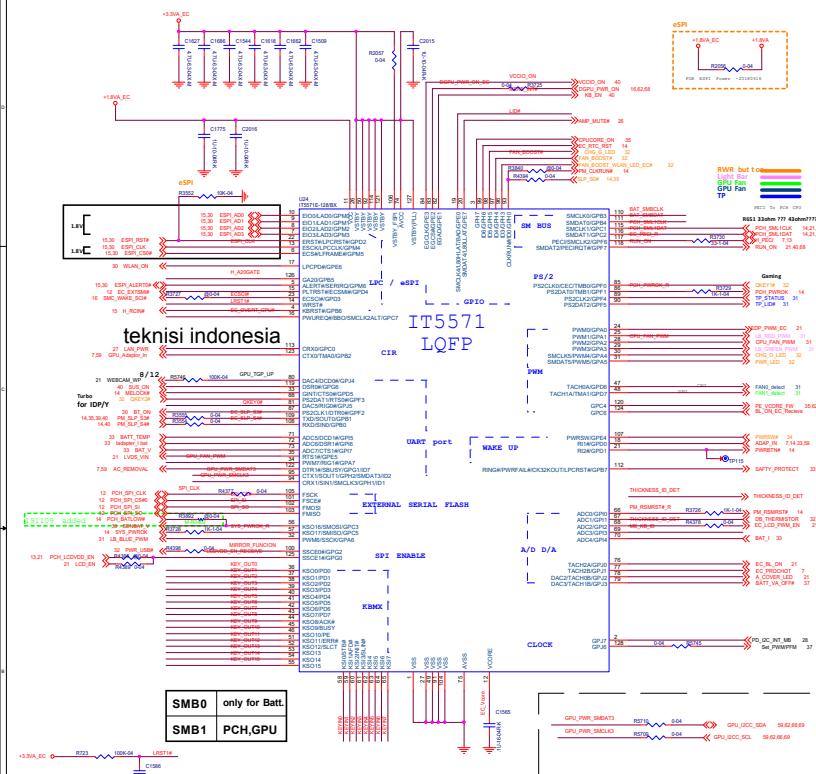


www.DeviceDB.XYZ - schematic, boardview, bios dump

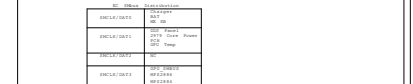
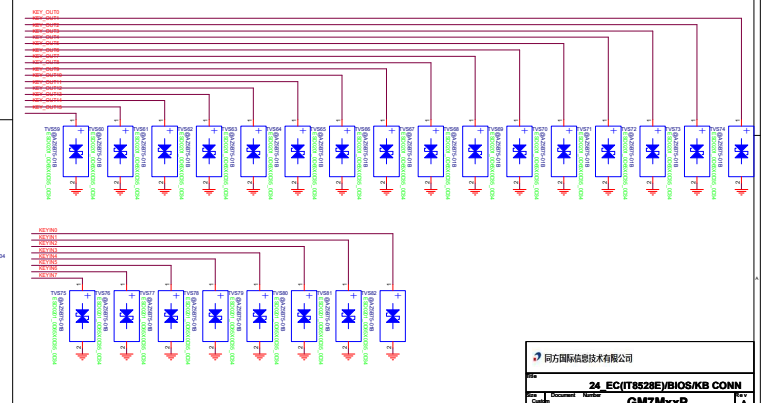




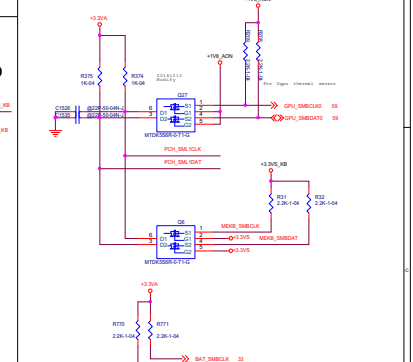




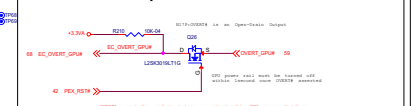
## ESD



## EC SMBUS LEVEL SHIFT



## GPU Over Temperature Protection





D

D

C

C

B

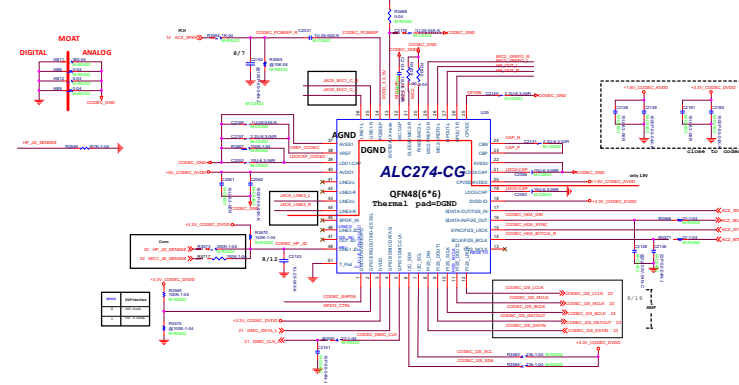
B

A

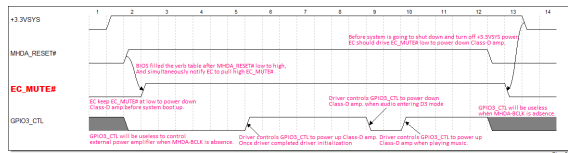
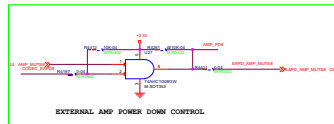
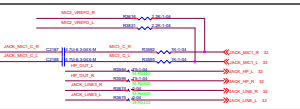
A

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Title		25 ME KB ESD	
Size A	Document Number		Rev A
Date: Tuesday, August 18, 2020		Sheet 25	of 70

**CODEC-ALC274**[illegible]

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## AMP-ALC1306

3.2V

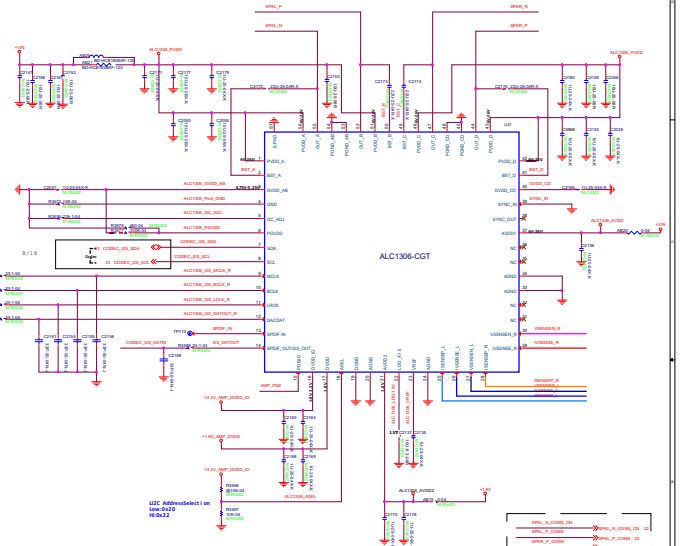
0.06

3.2V

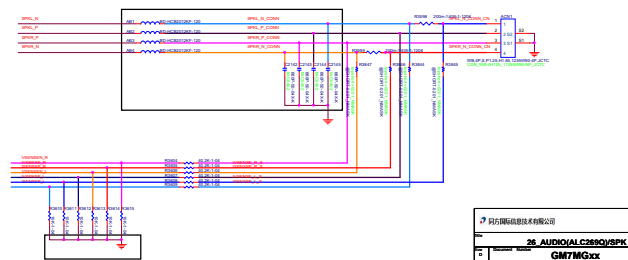
1.8V

0.06

1.8V



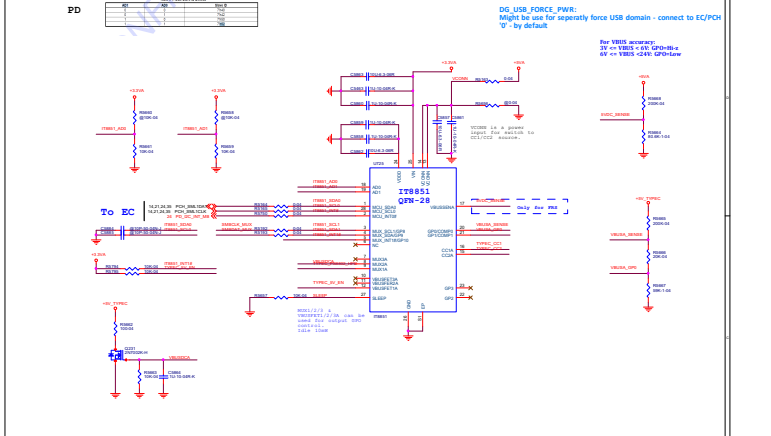
## INT\_SPEAKER



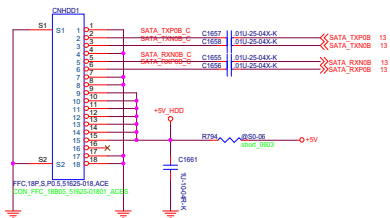
**LAN**

 同方国际信息技术有限公司			
Title			
27 LAN(RTL8125BG)			
Size	Document	Number	Rev
C		GM7MGxx	A
Date:	Tuesday, August 18, 2020		Sheet 27 of 78

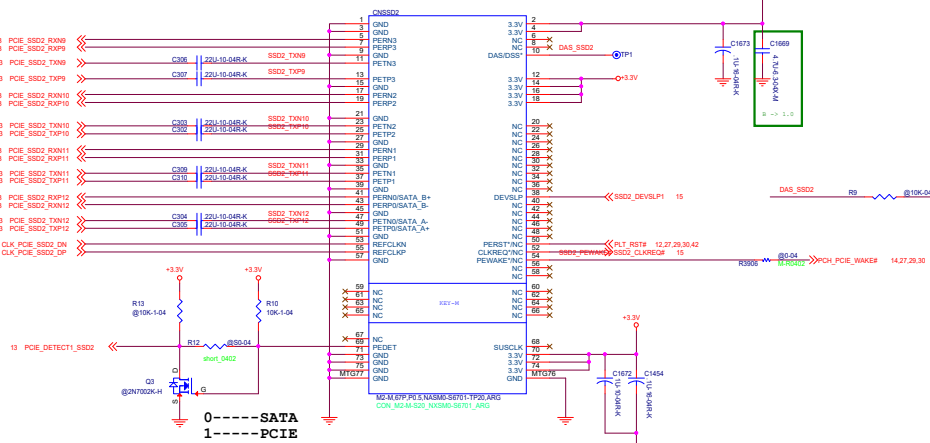
www.DeviceDB.XYZ - schematic, boardview, bios dump



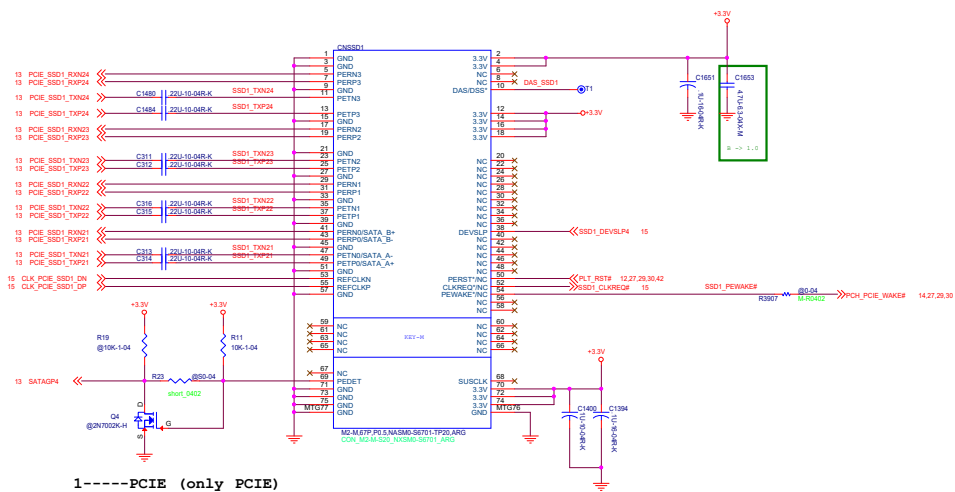
## SATA-HDD



## SSD2

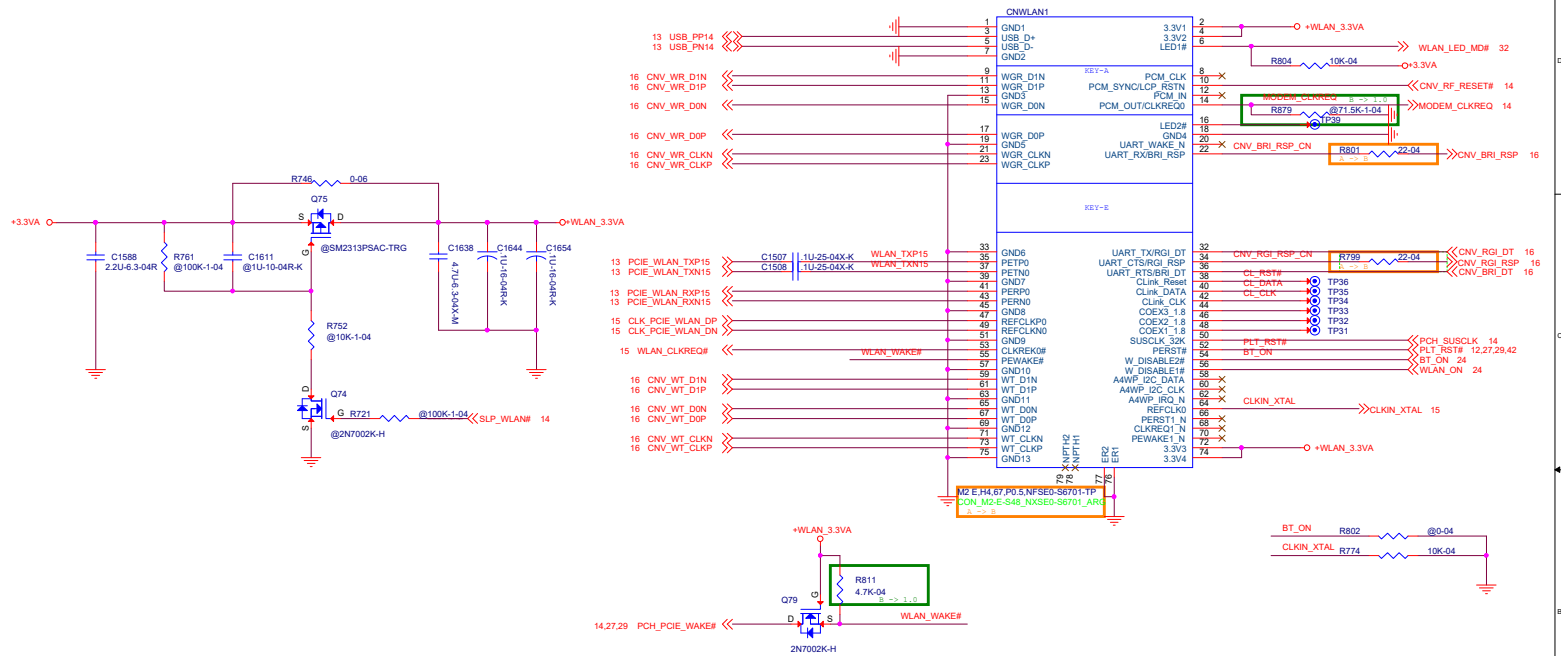


## SSD1

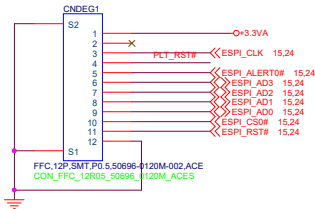


1-----PCIE (only PCIE)

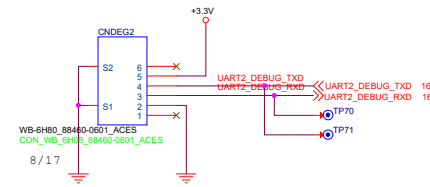
## WLAN CONN



## ESPI debug port



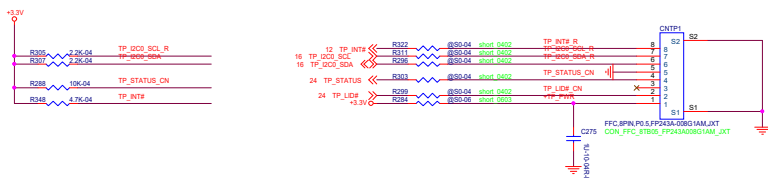
## UART debug port



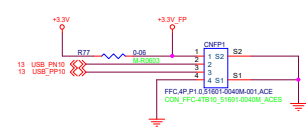
同方国际信息技术有限公司

30_WLAN/UART DEBUG/LPC DEBUG			Rev
Size	Document Number	GM7MGxx	A
Date:	Tuesday, August 18, 2020	Sheet	30 of 70

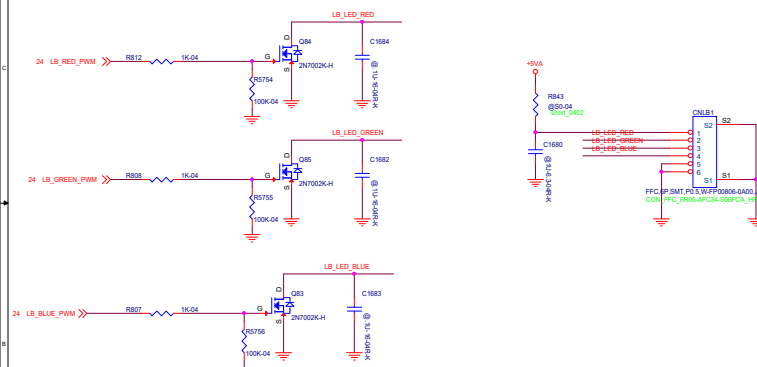
## Touch Pad



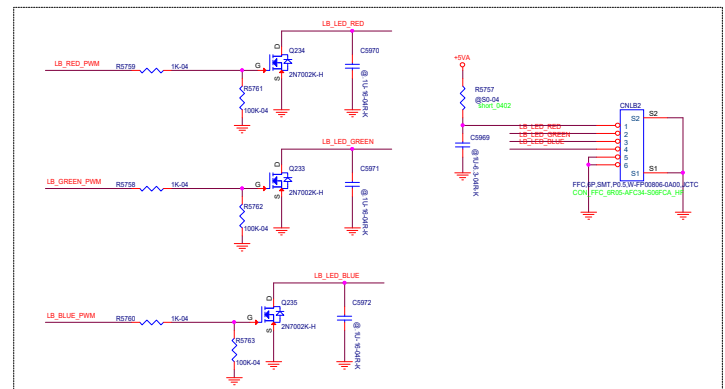
## Finger Print



## Light bar Control

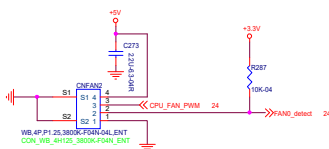


## Keyboard Backlight Control

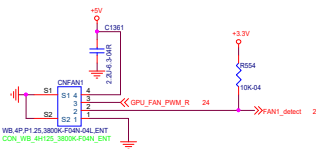


## FAN CONTROLLER

### CPU FAN



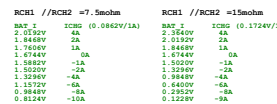
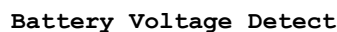
### GPU FAN



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Doc	Document Number	31_TP/CP/FAN/LB/FP	Rev
Comp	GM7MGxx		A
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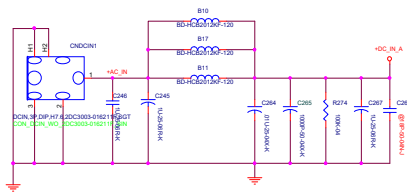






 同方国际信息技术有限公司			
<b>33_BATT IN/CHARGER(BQ24781)</b>			
Size	Document	Number	Rev A
Custom	<b>GM7MGxx</b>		

## +DC\_IN

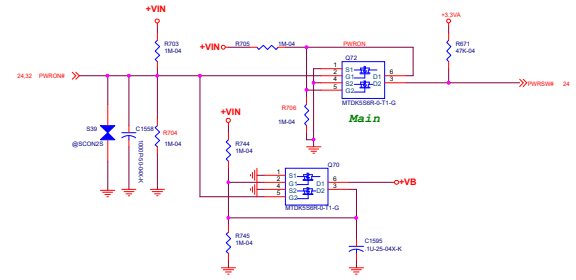


```

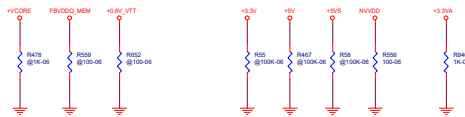
EMB20NP3V
ID=-13A TC=100 deg
Ipulse=-72A
Avalanche=-10A
9watt 1ms
15Watt 0.1ms

```

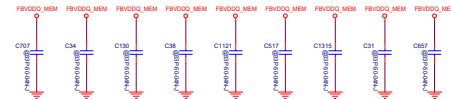
**POWER SW**



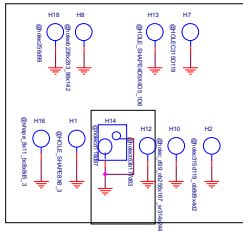
## Discharge Resistor



**For RF**



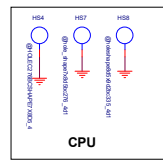
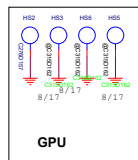
PCB HOLE



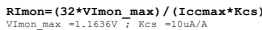
## WLAN HO



### THERMAL HOLE

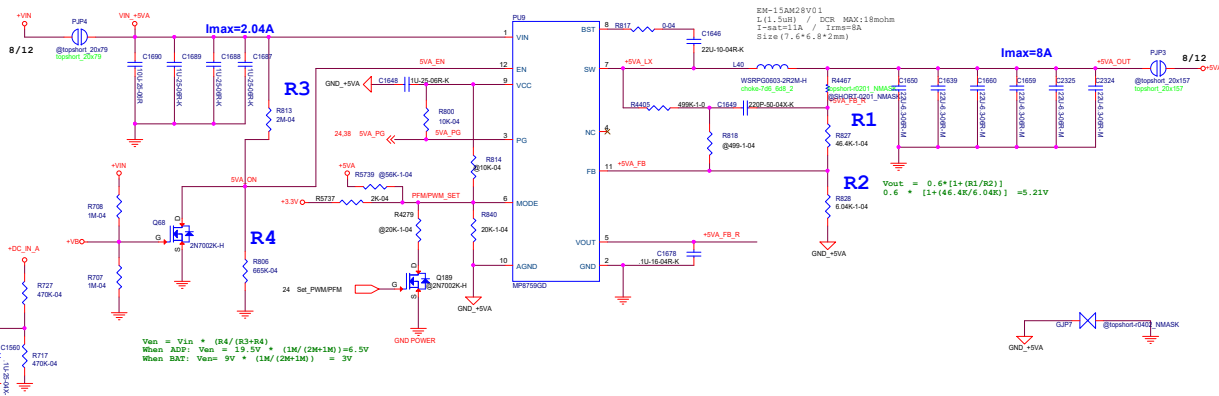


 同方国际信息技术有限公司			
Title			
34 DC IN/PWR_SW/H-S CAP/SCREW			
Size	Document	Number	Rev
Cuslom	GM7MGxx		A
Date:	Tuesday, August 18, 2020		Sheet 34 of 70

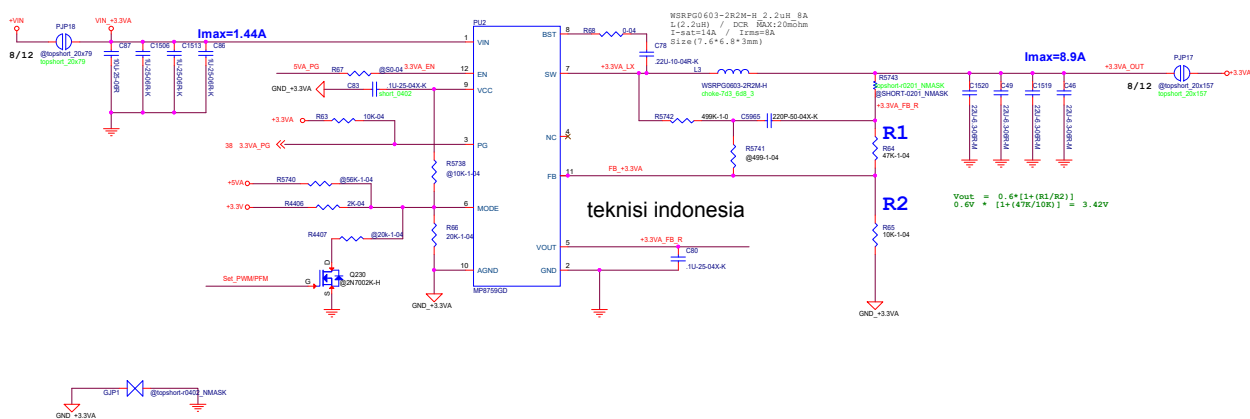




**+5VA**



**+3.3VA**

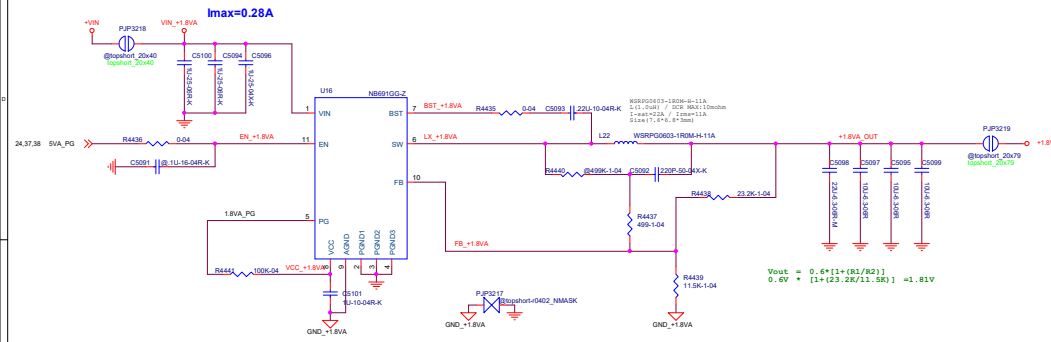


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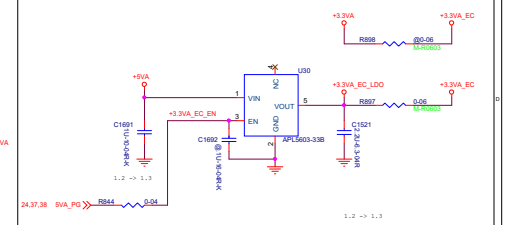
同方国际信息技术有限公司

Title				<b>37 POWER +5VA/+3.3VA</b>			
Size	Document	Number					Rev
Custom			<b>GM7MGxx</b>				A
Date: Tuesday, August 18, 2020			Sheet 37 of 70				

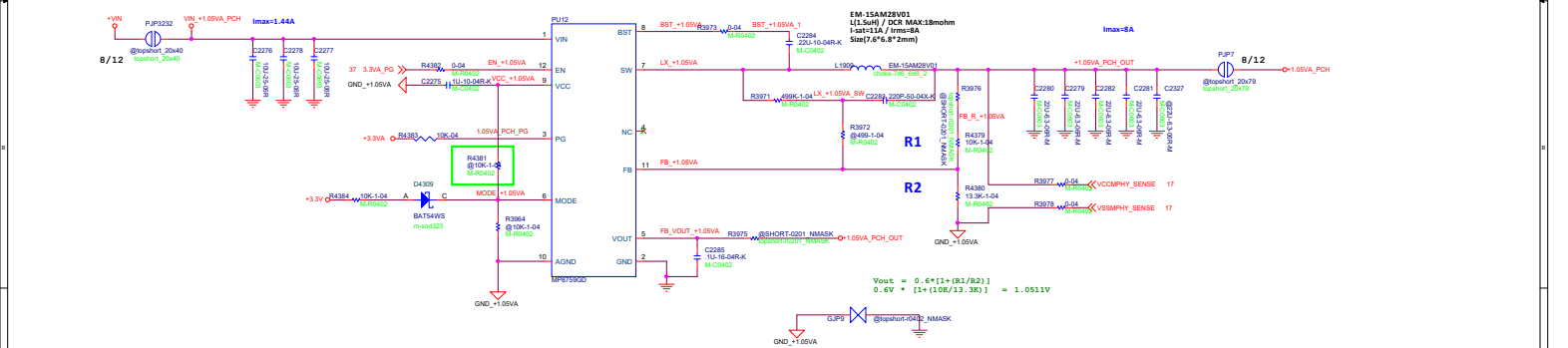
### 1.8VA Converter



### +3.3VA\_EC

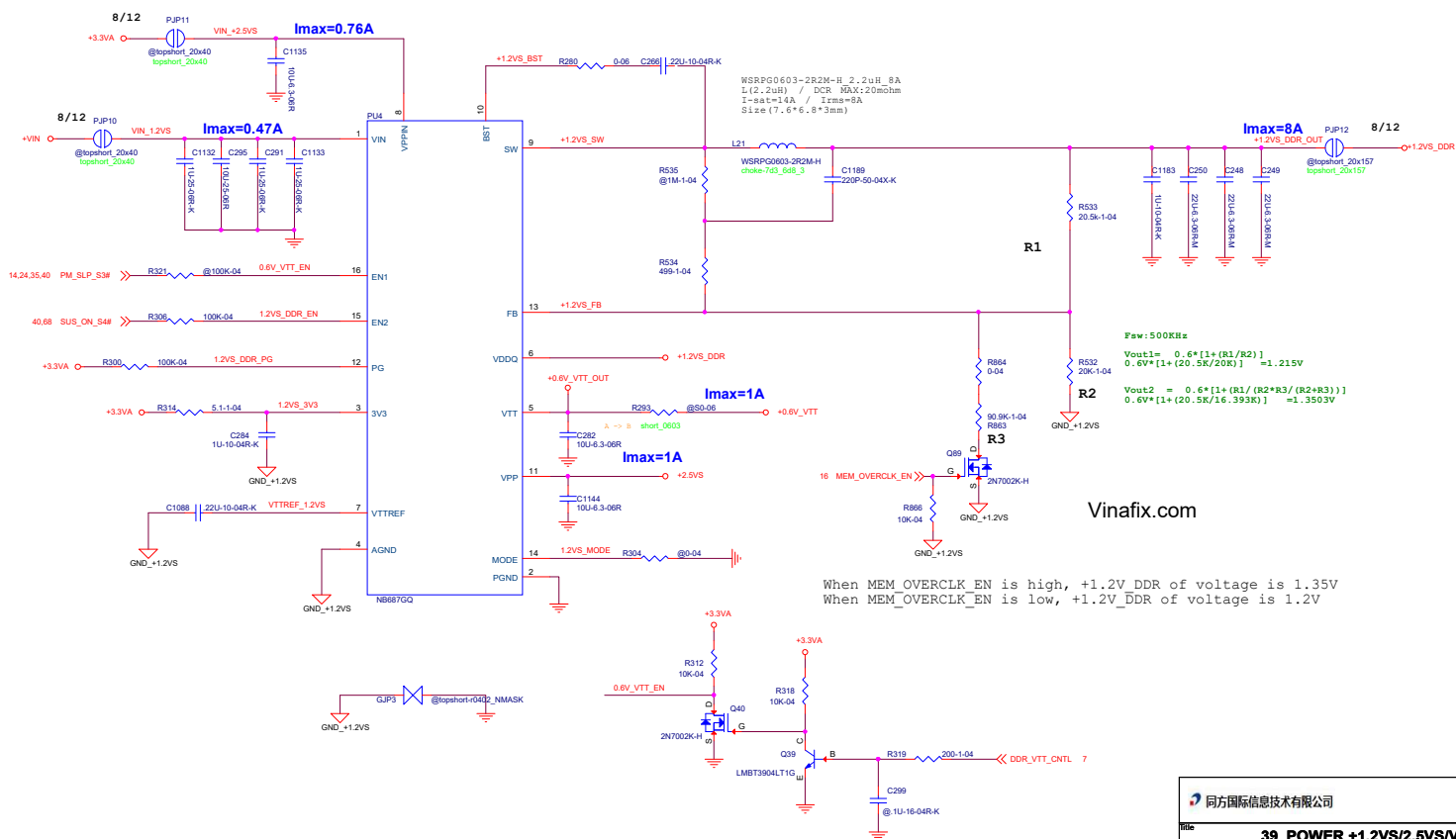


### +1.05VA\_PCH



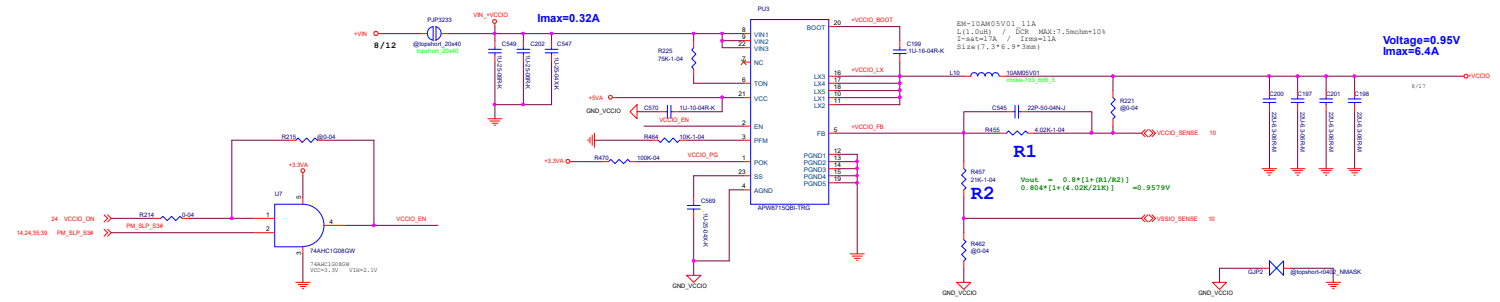
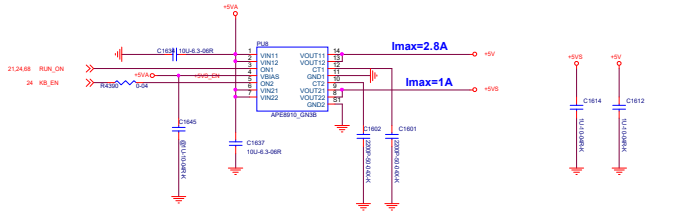
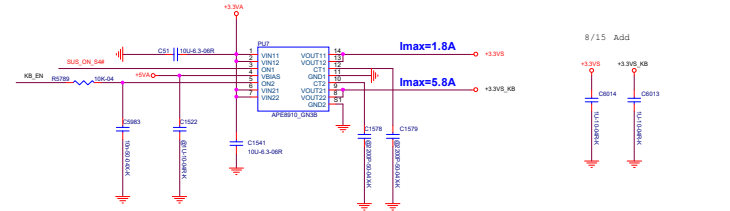
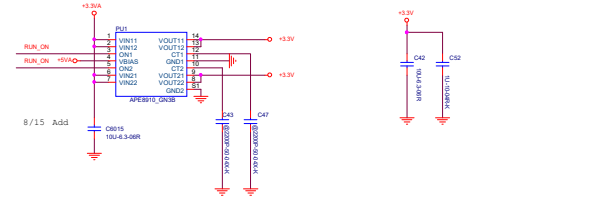
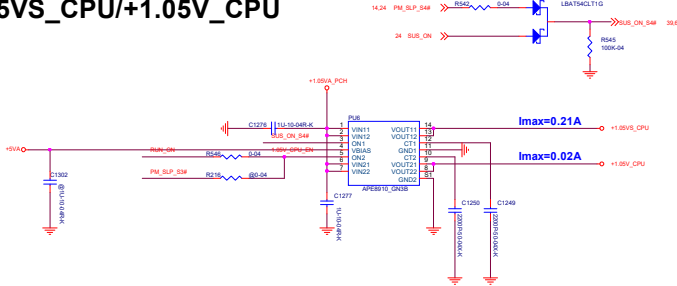
同方国际信息技术有限公司			
File	38_POWER +1.05VA_PCH+3.6_LCD		
Rev	Document Number	GM7MGxx	
Date	Version	Rev	A

**+1.2VS\_DDR/+2.5VS/+0.6V\_VTT**



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When MEM\_OVERCLK\_EN is high, +1.2V\_DDR of voltage is 1.35V  
When MEM\_OVERCLK\_EN is low, +1.2V\_DDR of voltage is 1.2V

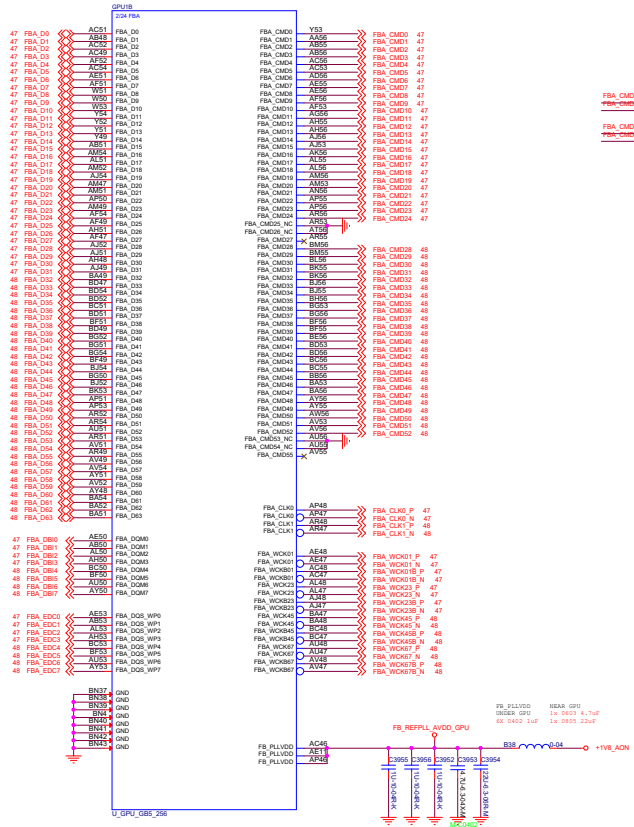
**+VCCIO****+5VS/+5V****+3.3VS/+3.3V****+1.05VS\_CPU/+1.05V\_CPU**

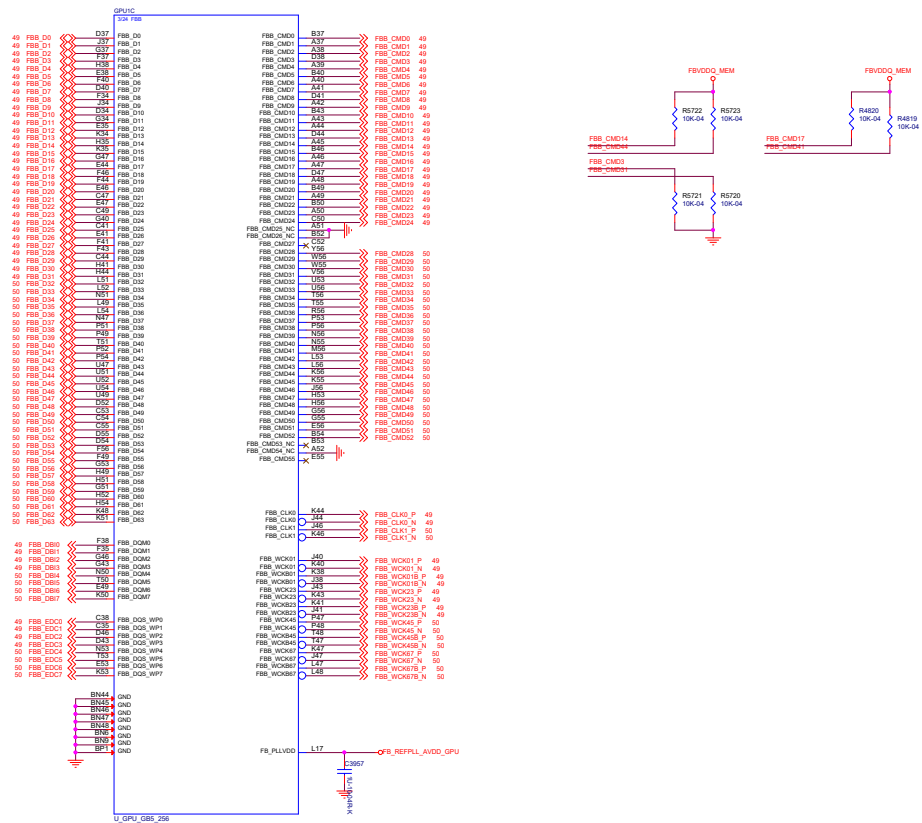
同方国际信息技术有限公司			
Doc	40_POWER +VCCIO+VS_PWR+V_PWR		
Rev	0	Customer Number	GM7MGxx
Date	November, August 18, 2020	Revise	00 of 78




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Title		
GPU N18E GFX-PCIE		
Doc	Document Number	Rev
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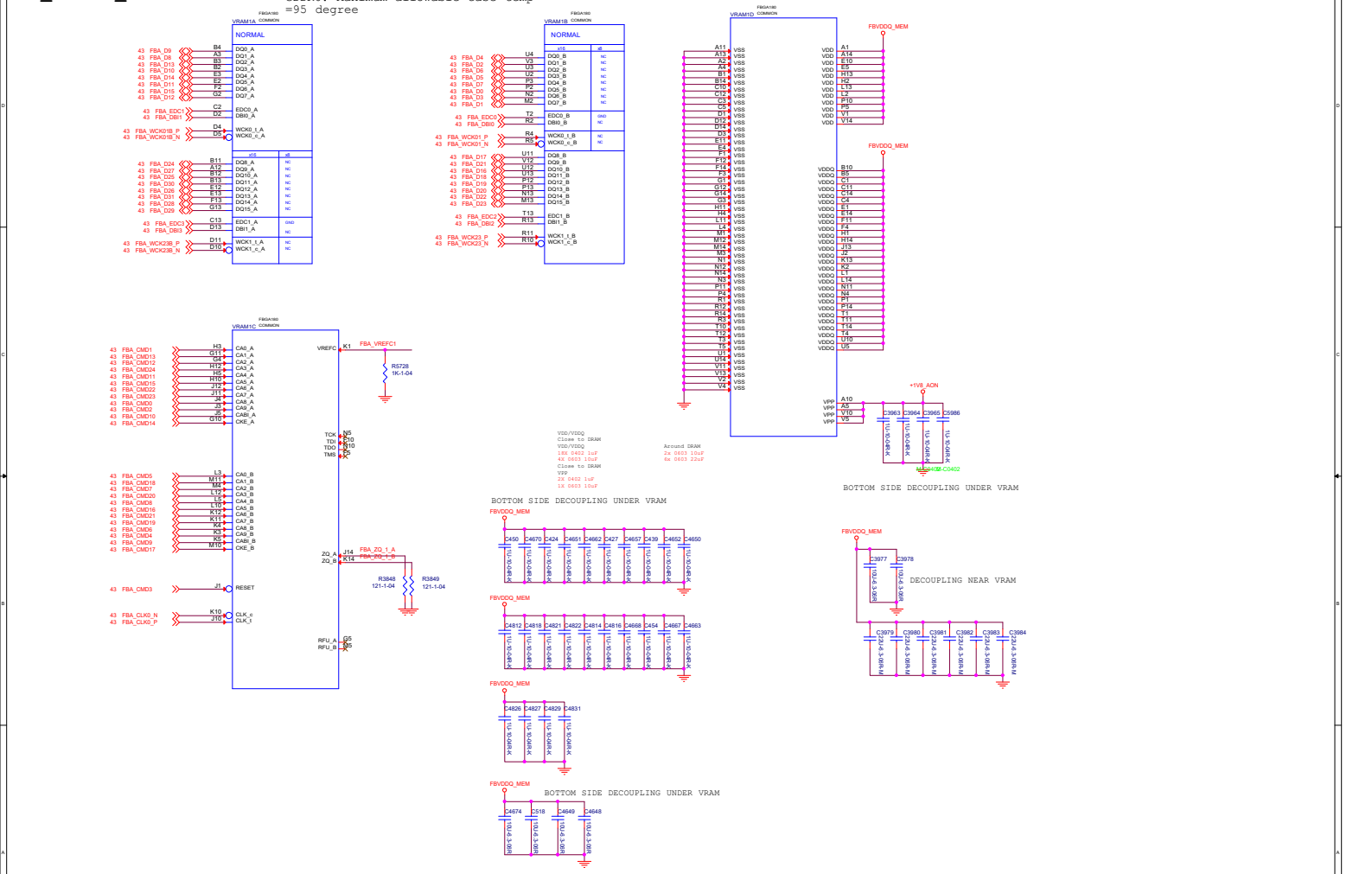




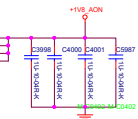
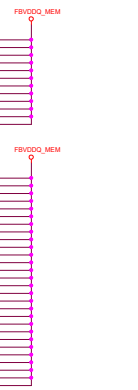
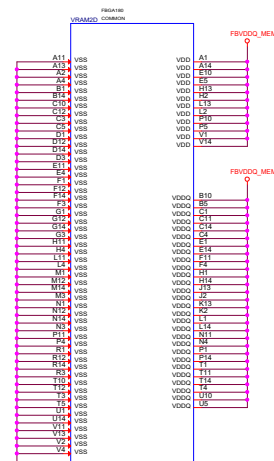
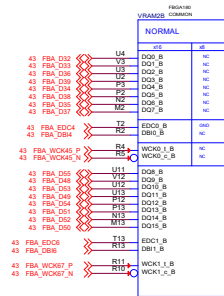
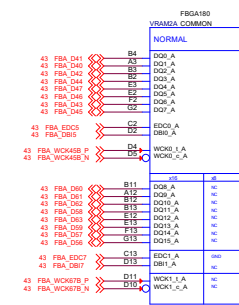
 同方国际信息技术有限公司			
Title			
GPU N18E Frame Buffer B			
Size	Document	Number	Rev
C		GM7MGxx	A
Date:	Tuesday, August 18, 2020		Sheet 44 of 72



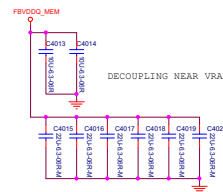




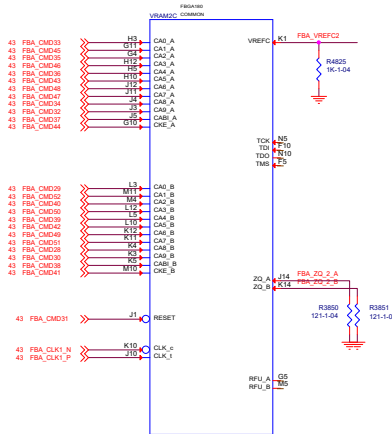
Maximum VRAM case Temp is 85 celcibus degree



BOTTOM SIDE DECOUPLING UNDER VRAM



DECOUPLING NEAR VRA



BOTTOM SIDE DECOUPLING UNDER VRAM

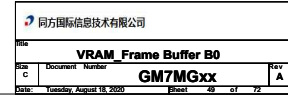
Close to DRAM	
VDD/VDDQ	Around DRAM
1X 0402 1uF	2x 0603 10uF
4X 0603 10uF	6x 0603 22uF
Close to DRAM	
VPP	
2X 0402 1uF	
1X 0603 10uF	

BOTTOM SIDE DECOUPLING UNDER VRA



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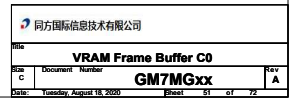


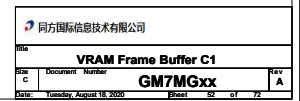


FBIQA180

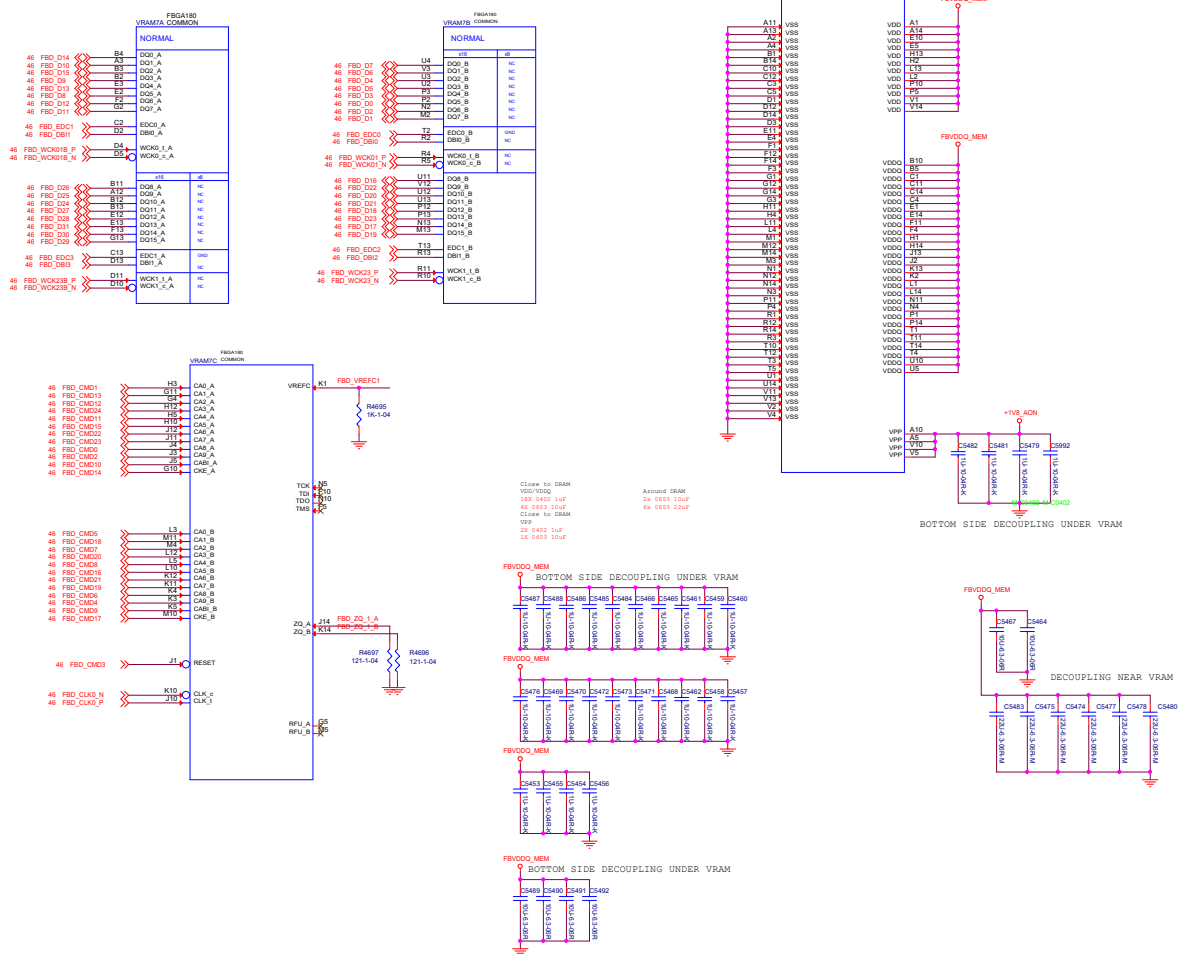


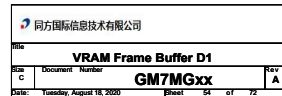
DECOUPLING NEAR VRAM

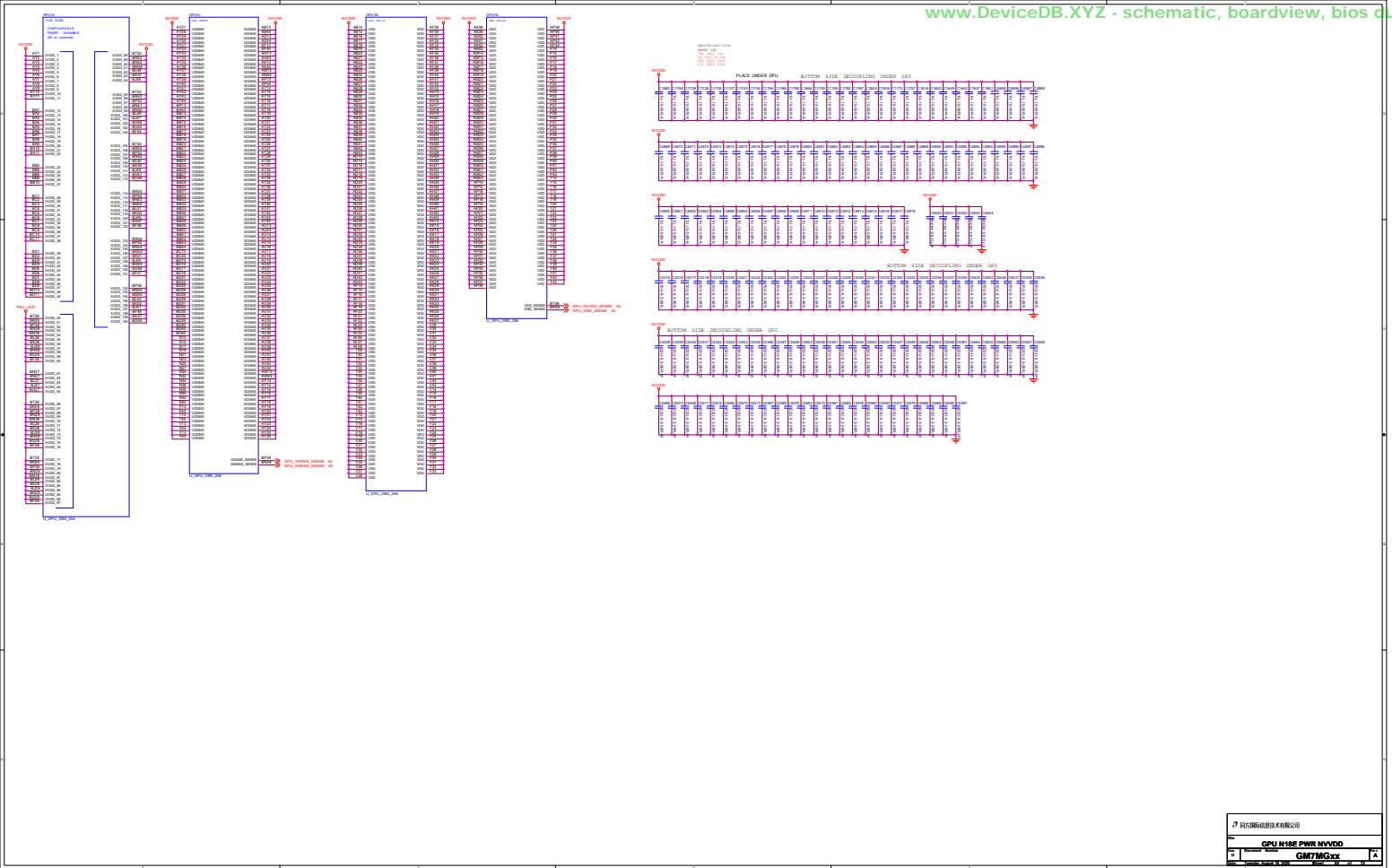




## MEM\_FBD[31\_0]













D

D

C

C

B

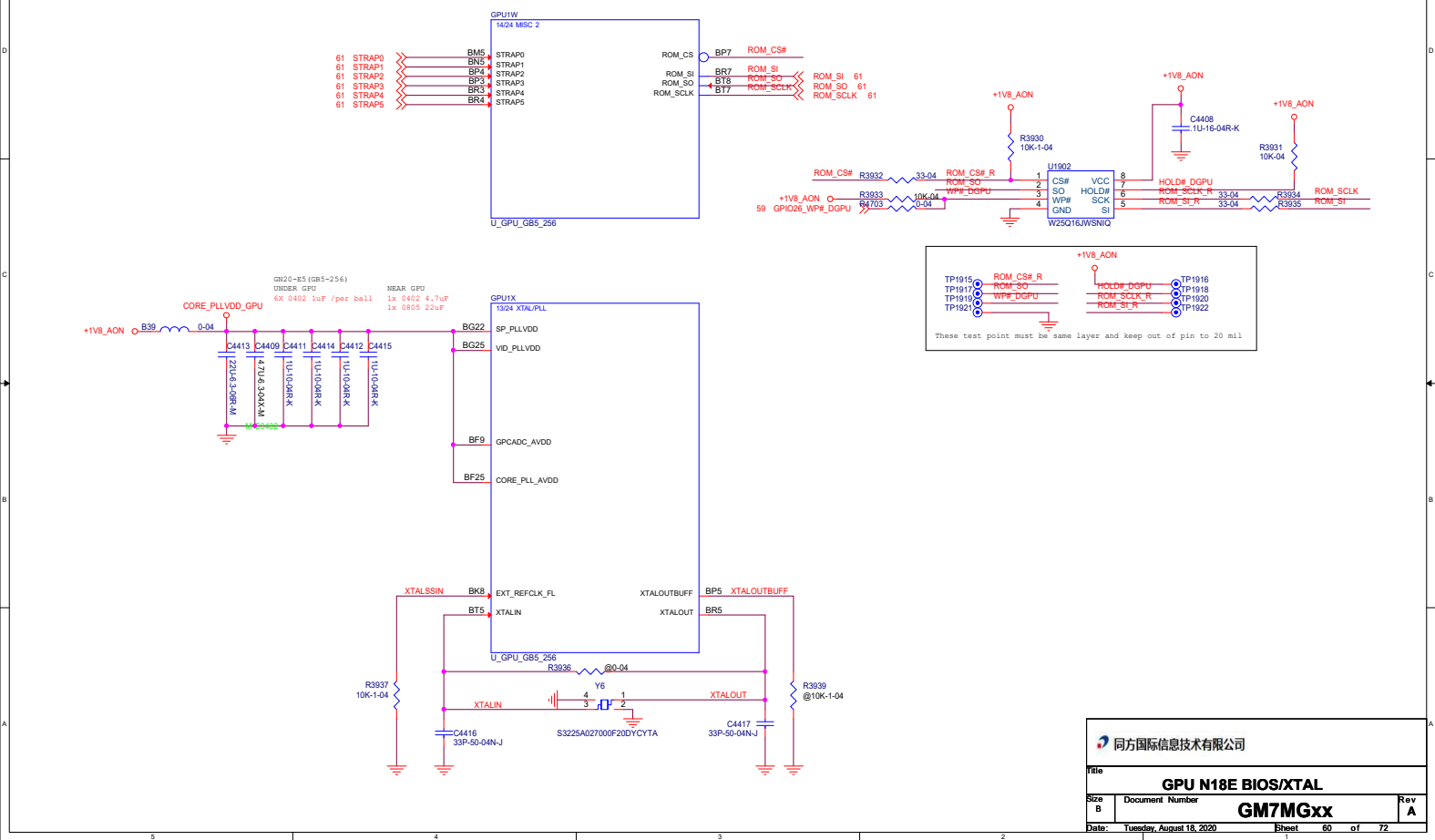
B

A

A

 同方国际信息技术有限公司			
Title			
GPU N18E NVLINK			
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Voltage(V)			
LEVEL	Min	Normal	Max
H	1.5	1.8	1.854
M	0.5	0.9	1.3
L	0	0	0.3
Invalid	1.3V<pin voltage<1.5V		
	0.3V<pin voltage<0.5V		

GN20-E5 GDDR6							
Density	Vendor	Part Number	Strap	Strap 2	Strap 1	Strap 0	
8Gb	Samsung	K4Z80325BC-HC14 C-die	0X0	L	L	L	
8Gb	Micron	MT61K256M32JE-14:A A-die	0X1	L	L	H	
8Gb	Hynix	H56C8H24AIR-S2C A-die	0X2	L	H	L	

Strap5,4,3 LH			
SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
0	0	0	1

Strap5,4,3 HLH			
SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
0	1	0	1

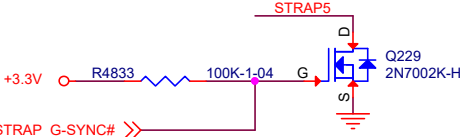
1:SMB\_ALT\_ADDR dual GPU alternate  
0:SMB\_ALT\_ADDR single GPU

1:DEVID\_SEL REBRAND  
0:DEVID\_SEL ORIGINAL

1:PCIE\_CFG reduced signal amplitude  
0:PCIE\_CFG normal signal swing

1:VGA\_DEVICE class code 300  
0:VGA\_DEVICE class code 302

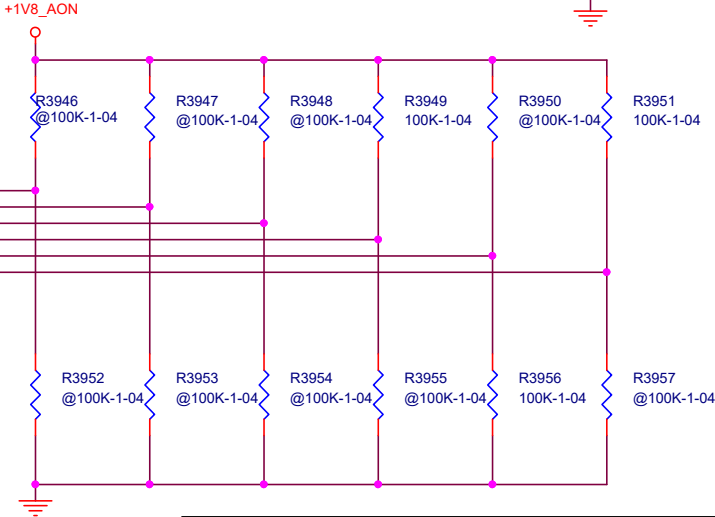
60 STRAP0  
60 STRAP1  
60 STRAP2  
60 STRAP3  
60 STRAP4  
60 STRAP5



FS OVERT			
FUNCTION	ROM_SO	ROM_SI	ROM_SCLK
disable	L	L	L
enable	L	L	H

60 ROM\_SI  
60 ROM\_SO  
60 ROM\_SCLK

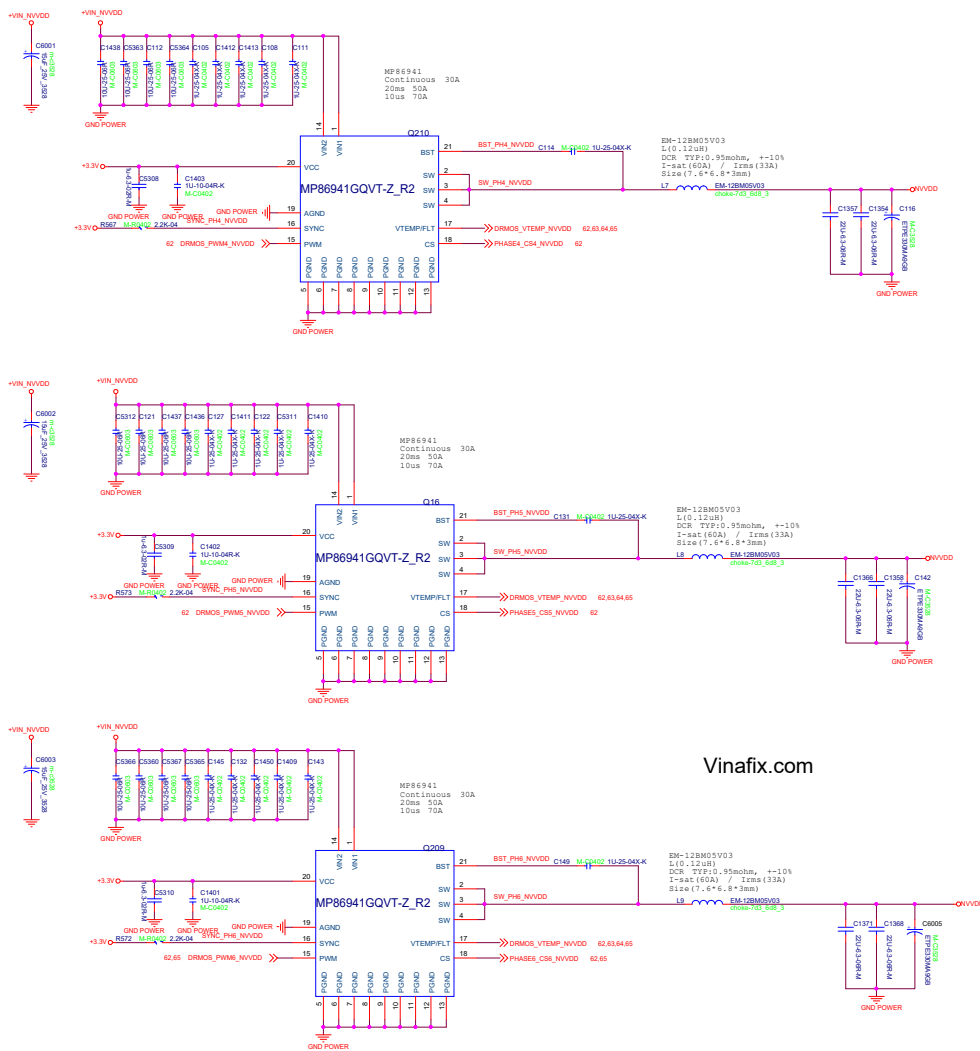
ROM\_SI  
ROM\_SO  
ROM\_SCLK



Title		
GPU N18E STRAP		
Size A	Document Number	Rev A
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Date:	Tuesday, August 18, 2020	Sheet 61 of 72



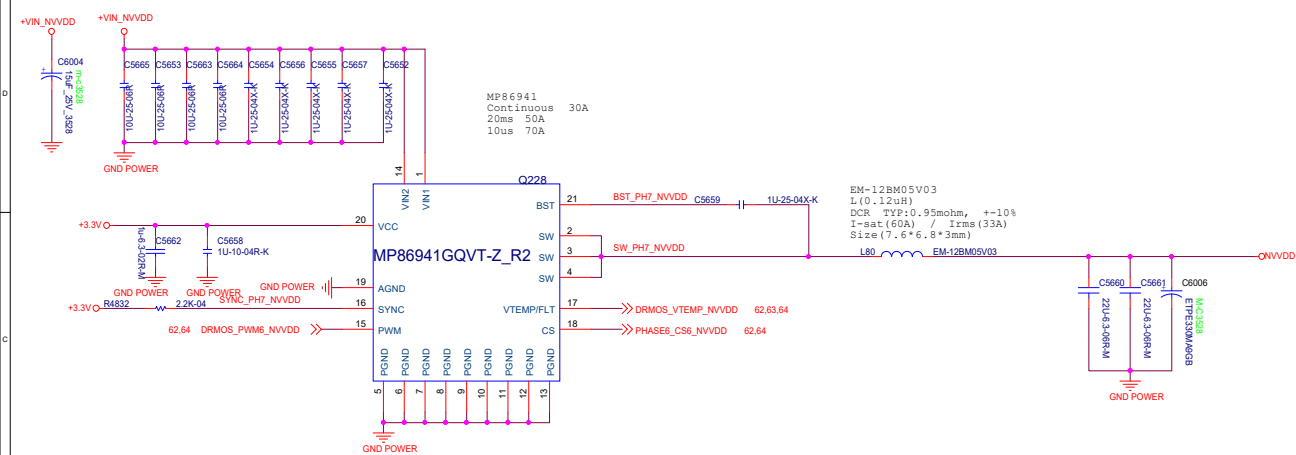




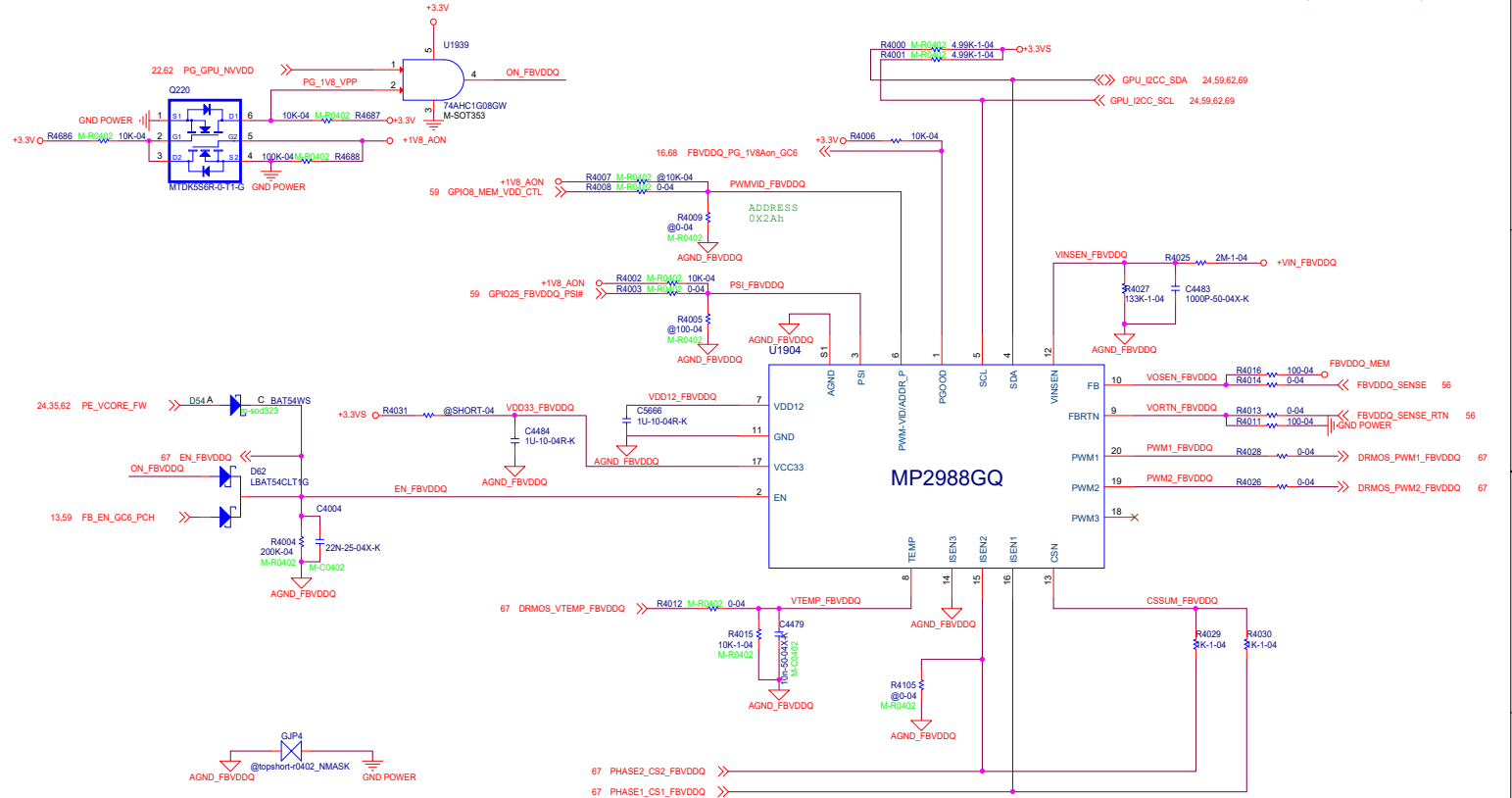
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POWER N18E NVDD 3PHASE_2/2			
Doc	Account	Number	GM7MGxx
Date	Thursday, August 16, 2006	Print	65 of 12

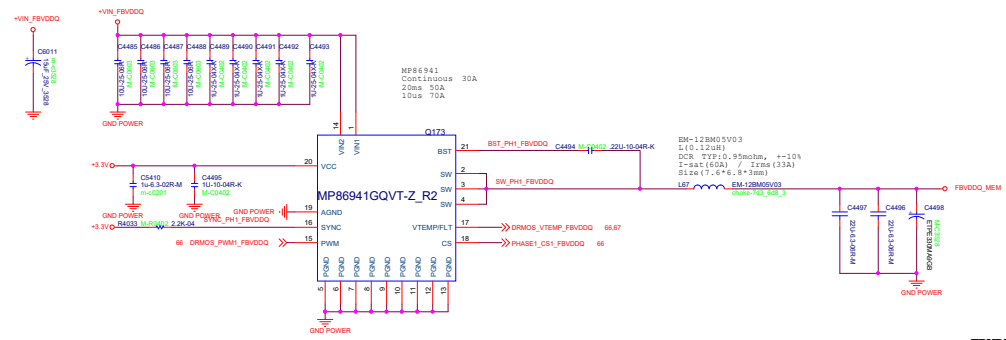




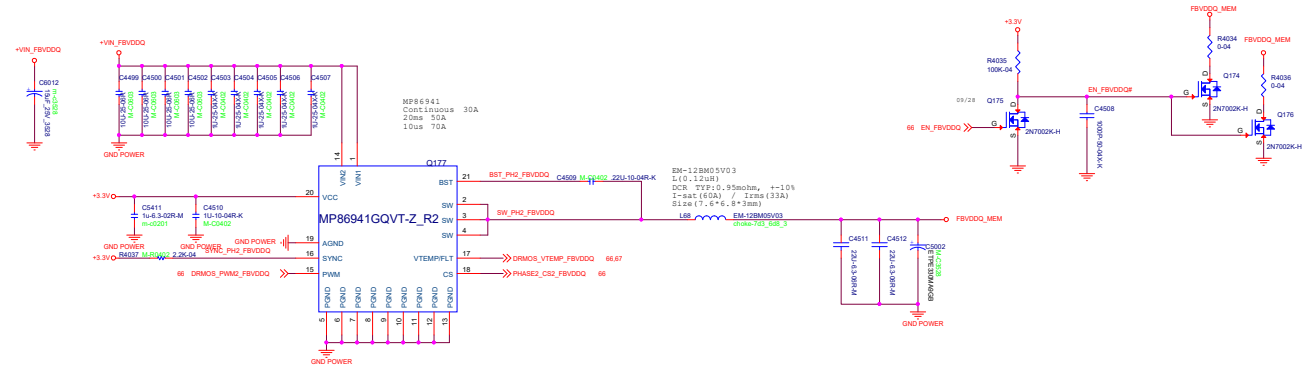
同方国际信息技术有限公司			
GPU POWER SEQUENCE			
File	Document Number	Rev	A
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File	POWER N18E FBVDDQ CONTROLLER		
Size	Document Number	GM7MGxx	Rev A
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## FBVDDQ\_MEM\_Discharge



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POWER N18E FBVDDQ 2PHASE			
Doc C	Document Number	GM7MGxx	Rev A
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Title			
POWER N18E PEX_VDD/1V8_AON			
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		GM7MGxx	
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PCB Version: A PCB P/N XXXX

No.	Modify Item	Modify Details	Schematic/Layout/BOM Change	Page
1	B1-1 Add capacitor for D05 AUXPANEL solved non-D05 LG panel no display	C8037,C9038	Schematic&BOM&Layout	27
2	B1-2 Change R723 value for DB thermistor	R723(10K to 47K)	Schematic&BOM	36
3	B1-3 Change R3651 value	R358(147K to 10K)	Schematic&BOM	36
4	B1-4 Changed power plane V18_AON to +3.3V_LCD for pull up	R4384,R4385	Layout	64
5	B1-5 Changed C443 value for ME interference	C4338to EEEH61E330L	BOM	46
6	B1-6 Changed U1908 PCB footprint	U1908	Schematic&Layout	72
7. Add jumper for power				
8. U2353 stuff				
9. R008 ROM should support MMC ; pending				
10. Modify I2C address				
11. M5744 (Stub to 100K)				
12. Add C6511&C6512				
13. Del U009,U01001,PC1&PC2				
14. U1908&U1909 exchanged Pin				
15. Changed M10&M1000 PCB footprint				
16. Del R2003&R10				
17. Add media_upgrade_nomenclature				
18. Modify CPU power V18 input capacitor stuff/delete				
19. Add new input output manual n				
20. Del U2002				